Electronics®

Circuit Designer's Casebook

Published by Electronics—1221 Avenue of the Americas, New York, N.Y. 10020

McGraw-Hill Books for Electronics Engineers

CHARACTERIZATION OF SEMICONDUCTOR MATERIALS

By PHILIP F. KANE, ***Director,*** **and**
GRAYDON F. LARRABEE, ***Manager, Compositional Methods Branch, both of Central Analysis & Characterization Laboratory, Texas Instruments, Inc.***

333 pages, 221 illustrations

Requiring no special knowledge of semiconductor technology, this comprehensive one-of-a-kind volume brings you a wealth of practical information for the evaluation and application of semiconductor materials and characterization techniques. Geared to meet the needs of all professionals, this unique guide provides a brief account of semiconductor development, then presents a concise nonmathematical analysis of the band theory. Semiconductor principles, bulk material characterization, single-crystal growth, chemical and physical imperfections in single crystals, epitaxial films, diffusion, and thin films are among other topics discussed.

SOURCEBOOK OF ELECTRONIC CIRCUITS

By JOHN MARKUS, ***Manager, Information Research, McGraw-Hill Inc.***

896 pages, 8½ x 11, over 3000 illustrations

A virtual desk-top retrieval center for engineers, designers, and technicians in all areas of electronics, this first book of its kind contains over 3,000 electronic circuits, complete with values of all components. A distillation of circuit knowledge for the past ten years, it brings together material from many diverse sources. The majority of circuits shown are recent semiconductor designs, but important electron-tube circuits are adequately represented. Included with each circuit is a concise description of its significant features, performance data, and operating characteristics so you can find the circuit that most closely meets your needs in any practical, on-the-job situation. It also tells you where to get further information on each circuit.

THE NEW ELECTRONICS

By BRUCE SHORE, ***Administrator of Scientific Information, Radio Corporation of America***

254 pages, 85 photographs

Today's solid-state revolution—from the discovery of the transistor in 1948 — is discussed in this "how-it-works-and-where-it-came-from" guide. It takes you into the laboratories where the great discoveries were and are being made, and explains in everyday language exactly what is happening. Completely up to date, the book offers you a rapid understanding of solid-state electronics and the phenomena associated with it — shown not only in all their beauty and spirit of adventure, but in their growing centrality to industrial and individual life. Illustrated with scores of photographs, the book offers full historical background from the ancient Greeks to the dedicated men and women involved in the field today.

HANDBOOK OF SEMICONDUCTOR ELECTRONICS, Third Edition

Edited by LLOYD P. HUNTER, ***Professor of Electrical Engineering, University of Rochester,*** **and prepared by 17 top specialists**

1,100 pages, 963 illustrations and tables

Everything you need to know about semiconductor circuitry is clearly explained and illustrated in this practical book. A now-famous work, it brings you step-by-step guidance in device physics, fabrication techniques, evaluation methods, and circuit design techniques in a single volume. Written by specialists who were chosen for their proven knowledge, ability, and experience, the book includes all recent advances to keep you abreast of today's rapidly developing integrated circuit techniques. In this new edition, a section has been added on the design of integrated operational amplifiers, and also a section dealing with the utilization of computers. Page after page of illustrations and tables offer visual clarity to every key aspect of semiconductor circuitry, and the entire book has been completely expanded, updated and revised.

AN ILLUSTRATED GUIDE TO LINEAR PROGRAMMING

By SAUL I. GASS, ***Vice President, World Systems Laboratories, Inc.***

224 pages, with charts, graphs, and drawings

In this excellent nontechnical introduction to an important new tool for solving business problems, the author draws on a wide variety of actual situations to show you just exactly what linear programming is, what it can do, how it is applied, and what kinds of problems it can handle for you. The search for the best solution — the optimum solution — has intrigued man throughout the ages, and this new, completely authoritative but thoroughly entertaining new book offers you all essentials of a key element in management today. Moving logically from the simple (getting dressed each day) to the most sophisticated levels of linear programming, the book is an admirable springboard for more advanced work and study in the entire fascinating field.

INTEGRATED CIRCUITS

Design Principles and Application

Prepared by THE ENGINEERING STAFF, MOTOROLA, INC., Semiconductor Products Division

385 pages, 7⅛ x 9⅞, 298 illustrations

With the help of this authoritative guide you can easily apply the valuable know-how of over twenty outstanding circuit design engineers to your own daily design problems. It gives a unified treatment to all phases of integrated circuits, clearly and precisely defining every important point from initial material processing to device packaging and reliability testing. You'll find in it detailed information on such subjects as acceptor doping . . . hole-electron spin assymmetry . . . recombination and generation . . . the gaussian distribution . . . diffusion time . . . sheet resistance . . . and much more.

SOLID-STATE ELECTRONICS

A Basic Course for Engineers and Technicians

By ROBERT G. HIBBERD, ***Semiconductor-Components Division, Texas Instruments Incorporated***

164 pages, 7 x 10, 90 illustrations

This unique work presents the principles of semiconductors in an unusual way. It starts with a description of semiconductors and their properties, the p-n junction and the junction transistors, and the characteristics of transistors and basic transistor amplifier circuits. It then describes the manufacture of transistors and other semiconductor materials and devices. The book also discusses the whole family of semiconductor devices and examines the applications of integrated circuits. Down to earth in presentation, it can be used by non-technical readers to obtain a working familiarity with the subject.

HANDBOOK OF THIN FILM TECHNOLOGY

Edited by LEON I. MAISSEL, ***Manager, Thin Film Basic Studies,*** **and REINHARD GLANG,** ***Manager, Device Process Studies, both IBM Components Division, East Fishkill, New York***

1,216 pages, 887 illustrations plus charts and tables

This all-inclusive reference work offers you today's latest and most dependable source of guidance on thin film theory and practice. The volume serves both as an introduction to the field and a practical day-to-day guide for scientists engaged in thin film work. Profusely illustrated, it gives you easy access to all information you need, helping you to catch up with the fast-moving field. Each of the 23 detailed sections has been written by a recognized authority who covers the subject areas he knows best. Divided into four sections: Preparation of Thin Films, The Nature of Thin Films, Properties of Thin Films, and Applications of Thin Films (this latter section with particular emphasis on thin films in the electronics industry).

See additional titles and ordering information on back cover

Electronics Circuit Designer's Casebook

Published by
Electronics
A McGraw-Hill Publication

14-A
Price $4.00, Printed in U.S.A.

All material copyrighted by
Electronics
McGraw-Hill, Inc.
1221 Avenue of the Americas,
New York, New York 10020

Table of Contents

MEASUREMENT

Fast-discharge sawtooth simplifies capacitance meter 1
Logic signals pulse heaters for multiplexed display 16
Analog-digital circuit turns scope into curve tracer 19
FET supply tests bipolar current gain 25
Hitch in time saves gates in 12-hour digital clock 57
Any voltmeter reads electronic thermometer 61
Supply tester outdoes scope as ac noise meter 69
Amplifiers let voltmeter measure op amp noise 73
FET pair bridges meter impedance gap 74
Simple photocell circuit measures pulsed laser power 81
Voltage monitor is easy on both battery and budget 91
Op amps find values of buried resistors 98
Preset pulse train checks sequential logic 111
Switch oscillator controls four-wire resistance checks 116
Q-multiplier analyzes audio-frequency tones 124
Comparator increases rate meter's response 126
Feedback circuit checks thermal resistance 144
Resistors come to light in digital display system 154

POWER SUPPLIES

Low-voltage regulator uses reversed error amplifier 10
Comparator logic limits switching regulator current 13
Diode and SCR protect multiple-voltage equipment 22
Shorted load folds back supply current 45
Four-layer diode circuit out-regulates zener by 5:1 47
Probability analysis cuts power supply needs 54
Low-voltage feedback loop controls high-voltage supply 62
Op amp splits supply for other op amps 67
SCR crowbar circuit protects Impatts 77
Battery discharge triggers alarm and shuts off supply 80
Regulator gives overvoltage protection for TTL 82
Optoelectronic switch monitors line power 86
Op amps form self-buffered rectifier 93
Monitor teams spare gates and solid state lamps 97
Diodes prevent power loss and burnout in converters 101
Flashlight helps monitor voltage levels 105
Diode-switched FETs rectify the full wave 110
IC oscillation sets up a mini-sized bias supply 114
Switching regulator drives ICs and Nixies off battery 115
Dc-to-dc converter offers positive or negative bias 125
Short-circuit protection for voltage regulators 130
Capacitors add up in voltage multiplier 141
A dynamic load tester for regulated power supplies 147

FILTERS

Resistance change alters filter's output function 30
Tunable active filter maintains constant Q 37
Versatile digital circuit filters highs, lows, or bands 46
Impedance-lowering op amp speeds filter response 56
Active RC network has two movable zeros, fixed poles 60

COMPARATORS AND DETECTORS

High-impedance driver boosts detector's dynamic range 18
Light-emitting diode pair forms null indicator 33
Detector measures phase over full 360° range 38
Nonlinear logic detects voltage tolerance levels 66
Digital bidirectional detector keeps the count honest 83
FET phase detector can be frequency-voltage converter 112
Exclusive-OR ICs serve for phase-locking tasks 118
Signal detector operates from 5-volt supply 136
Shift register simplifies design of phase comparator 151

CONTROL

Digital phase shifter maintains quadrature 4
Voltage-frequency converter uses four-layer diode 7
A-d converter provides real-time error correction 9
Transistor matrix driver supplies varying loads 14
Feedback zeros dc level of diode gating circuit 28
Short-delay J-FET switch gates high-speed data 41
Flip-flop pair synchronizes pulses and floats clocks 51
Stable FET clamp operates at 10 MHz 55
Gate suppresses pulses from switch contact bounce 64
Counter shifts signal phase only one way 70
Series limiter tracks signal, finds symmetry 71
Op amps delay and shape data signals 72
IC limiter preserves phase over 50-dB dynamic range 85
Single IC pulser eliminates contact bounce 88
Zener diodes reset sampling gate automatically 89
Shared one-shot simplifies pulse width converter 100
Fail-safe flame sensor provides control functions 102
Low-cost digital ICs prevent operator errors 106
Storage coil cuts relay pull-in delay 108
Variable FET resistance gives 90° phase shifts 113
Zeners cut corners in MOS gate driver 117
Dynamic braking emf signals motor to reverse 119
Telemetry signal conditioner centers its slicing level 121
Comparator and ac coupling provide dc transformer action 122
'Make-before-break' mode improves FET switch 129
Unijunction device eliminates contact bounce 132
Bridge circuit relies on common ground 133
Negative impedance stabilizes motor's speed 135
Inverted-mode transistors give chopper low offset 137
Two MOSFETs form transient-free linear gate 139
DTL/TTL controls large signals in commutator 140
Variable dc input adjusts pulse width over wide range 143
Zener diode in op amp's loop enables symmetrical clipping 145
ICs gate FETs for roll rate data 145
P-i-n diode T switch consumes little power 148
Op amps reject line noise in a-d converter's input 153

GENERATION

Resistance switching cuts tone oscillator jitter 2
Divide-and-sample loop cuts phase-locked VCO slippage 4
Hard-limited sinusoid eases frequency multiplication 11
FET current source gives stable, precise ramp 15
Dual op amp comparator controls ramp reference 23
One-shot makes fast trigger out of slow input pulse 24
Feedback pot extends multivibrator duty cycle 26
Variable pulse generator consists of four inverters 27
Low-frequency oscillator uses subharmonic sync 27
Triggered sweep generator responds to 100-ns spike 31
Broadband pulse generator uses small timing capacitance 32
Widerange multivibrator costs just 25¢ to build 34

IC frequency doubler runs at logic speed 35
Variable oscillator controls pulse width and spacing 42
Dual gate plus transistor generates 12 functions ... 50
High-voltage pulser spares battery supply 53
Voltage changes frequency of multivibrator by 10,000:1 68
Avalanching transistors speed-up high-voltage pulses 76
Wien-bridge oscillator needs only one op amp 78
One-shot saves power without losing time 79
Pulse generator uses digital ICs 90
Thermistor stabilizes Gunn oscillator 92
RF linear IC squares high-frequency sine waves .. 94
Stable unijunction VCO needs no critical components 95
Field effect transistor converts triangles to sines ... 103
Comparator and multivibrator add up to a linear VCO 107
Wave squarer shifts phase as much as 360° 109
Feedback triggers one-shot from both polarity edges 112
Monostable protected against 60-hertz pickup 127
One-shot generates wide range of periods 128
Two op amps simplify design of oscillator 131
Divider splits frequency into any ratio from 1 to 99 .. 133
A staircase and a ramp yield multiple sawtooths ... 142
Unijunction controls oscillator in simple underwater pinger 155

AMPLIFIERS

Instrument amplifier offers high gain 6
IC transistor array compensates for temperature ... 8
With feedback, isolation amp gives better-than-unity gain 21
Amplifier slew-rate curves simplify design decisions 43
Diodes stabilize FET gain to 1% over 100°C range . 48
Bootstrap boosts gain of low-noise rf preamp 52
High-voltage amplifier offers high frequency, too ... 59
Op amp's current booster ends crossover distortion . 63
Feedback amplifier speeds phototransistor's response 65
1-volt cell powers mini audio amplifier 75
Symmetry principle eases design of summing op amp 87
Optical biasing maintains phototransistor sensitivity 91
With some discrete aid IC op amp swings 100 V ... 96
Feedback limits amplifier better than zeners can ... 96
Matched FETs stabilize amplifier's bandwidth 123
Zener in bootstrap extends amplifier's range to dc . 138
Regulator holds temperature of chip's substrate constant 149
Diodes eliminate crossover distortion in video amplifier 150

LOGIC

Doubling the divisor yields odd-order counter 3
Interrupt register secures all data signals 7
Flip-flop sequences conversion register 12
Positive and negative gates trim logic package count 17
One-of-eight decoders test and correct parity 20
Fast ECL-to-TTL interface shifts data for 80¢ per bit 36
Counting by halves simplifies odd-order symmetric counter 39
Seven-code PCM converter clocks at data output rate 40
Gated clock cuts counter delay to 60 ns 44
Low-cost exclusive—OR needs no power supply ... 58
Sequential gate won't chop odd-length pulses 78
Wired—OR circuit simplifies binary number comparison 84
Control voltage resets logic at power turn-on 99
Single hex inverter picks data signals from noise .. 103
Build ring counters with standard MSI 120
IC line receiver converts pulses to logic levels 152

Foreword

Ask any electronics engineer if he could use another filter to work with and, after mentally ticking off such types as constant-k, m-derived, Chebyshev, Butterworth, active, L-C, and a host of others, he'd probably say: "Thanks, but no thanks. I have enough problems building the ones I know about." But there is another kind of filter every engineer needs desperately — an information filter.

Probably no one works closer to ground zero in the information explosion than the electronics engineer. How can he recognize and save the published material that's of lasting value, but only note and then discard the current news information that has a built-in obsolescence factor? Making these evaluations under the real-time pressures of completing a design project isn't easy.

Books like this one, we feel, will help him assemble a readily accessible storehouse of design information with a long shelf life. In this case, we have done the filtering.

This book is a collection of recently published basic, how-to articles from the technical article section of Electronics, combined with brief circuit ideas from the Designer's Casebook section. It can be used both as an up-to-date practical design textbook and as an idea book.

The editors of Electronics

Fast-discharge sawtooth simplifies capacitance meter

by R.W. Johnson
R.W. Johnson Co., Huntington Beach, Calif.

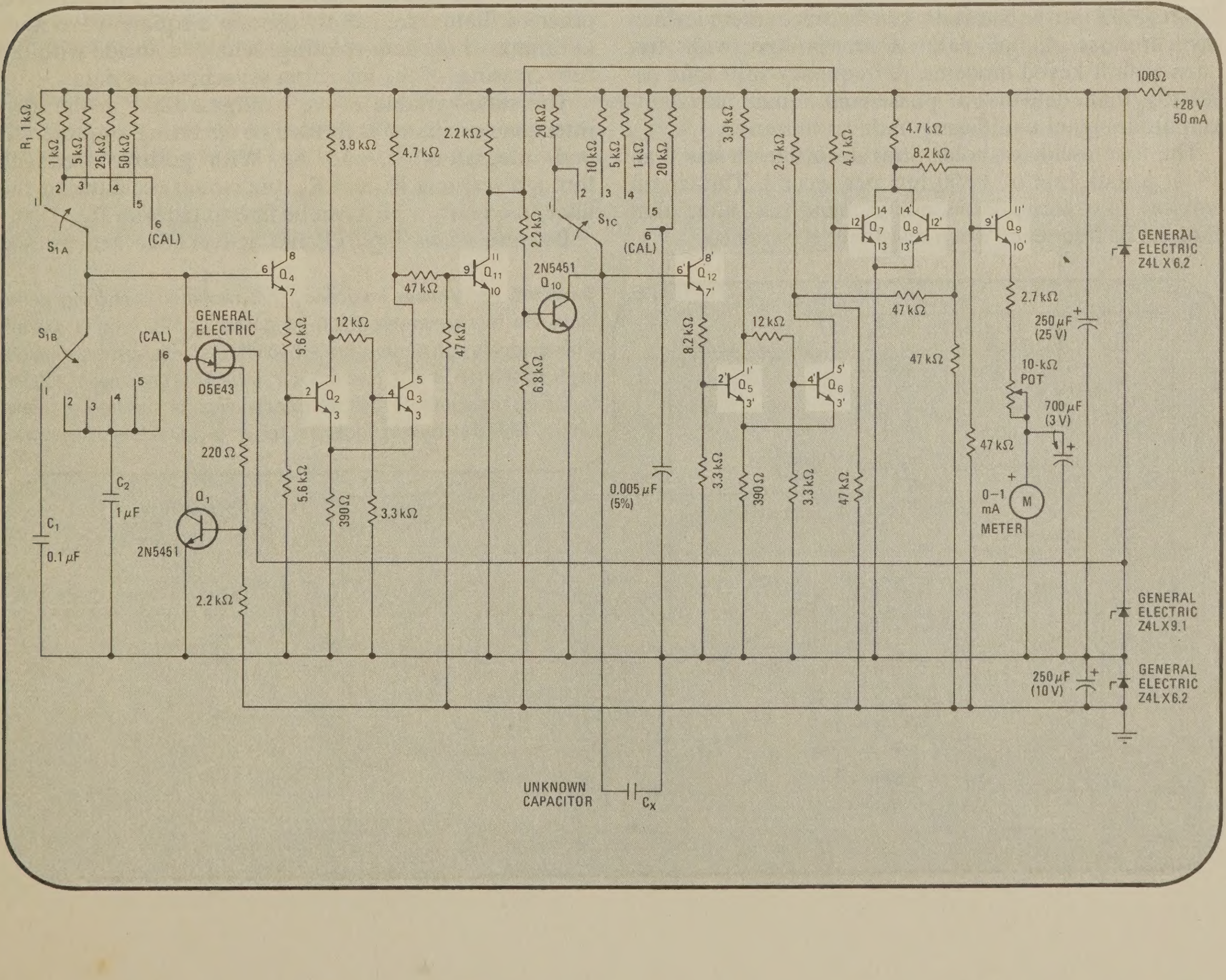
A direct-reading capacitance meter, accurate to 2%, employs a low-cost unijunction transistor to obtain a reference sawtooth voltage. The circuit measures a pulse duration proportional to the capacitance value to be determined. An average-reading meter is used to indicate capacitance directly on a linear scale. Measurement accuracy depends on meter movement and circuit calibration.

The relaxation oscillator portion of the circuit does not require a high-quality, expensive transistor to supply a reference voltage. A low-cost unijunction can be used, because high-current transistor Q_1 quickly discharges the oscillator's timing capacitor, dropping emitter voltage below its valley voltage and permitting a low-value timing resistor to be used. Since the second base (base 2) of the transistor is returned to a zener-regulated voltage that is lower than the charging voltage, the effects of leakage currents are minimized. Timing components are selected with the range switch, S_1.

The relaxation oscillator generates a sawtooth control voltage that discharges the unknown capacitor, C_x, once each cycle. To establish a reference voltage, the oscillator's output is applied to a Schmitt trigger formed by Q_2 and Q_3 through emitter-follower Q_4.

Capacitor C_x charges as the oscillator's timing capacitor charges from the regulated supply. When the voltage across C_x reaches the firing point of a second Schmitt trigger formed by Q_5 and Q_6, the trigger turns on, enabling the NAND gate formed by Q_7 and Q_8. The

Meter measures capacitance to 2%. Reference sawtooth generated by unijunction transistor relaxation oscillator and Q_2-Q_3 Schmitt trigger controls voltage across unknown capacitance C_x. Another Schmitt trigger (Q_5-Q_6) fires when voltage across C_x reaches its threshold, enabling Q_7-Q_8 NAND gate. Pulse duration of gate output is linearly proportional to C_x. Average-reading linear-scale meter shows capacitance.



gate output pulse, taken from the common collectors of Q_7 and Q_8, has a duration linearly proportional to the unknown capacitance.

Applying this pulse to an averaging meter through emitter-follower Q_9 allows the unknown capacitance to be read from a linear scale. Capacitor C_x discharges the instant the unijunction transistor fires, because high-current transistor Q_{10} conducts and remains saturated until the reference Schmitt trigger turns on again.

Even the true capacitance of leaky capacitors can be measured. The only condition under which the meter will give a false reading is when capacitor leakage resistance is less than 10 times the charging resistance. Since all the charging resistors have low values, most capacitors, including electrolytics, can be measured accurately.

Transistor Q_{11} performs as a pulse shaper and inverter so that Q_{10} can properly discharge C_x. Emitter follower Q_{12} drives the Q_5-Q_6 Schmitt trigger and prevents overloading C_x. Ten of the 13 transistors required for the circuit are housed in two integrated circuit packages—RCA's type CA3046 five-transistor arrays (shown in white with package pin numbers).

The capacitance meter has five full-scale decade settings, from 0.001 microfarad through 10μF. The smallest capacitance that can be accurately measured is about 100 picofarads because of stray capacitance as well as sawtooth rise and retrace times. Only precision resistors should be used for range switching. Resistor R_1 is trimmed to $C_2/10\ C_1$ kilohms so that capacitors with a tolerance of 10% or 20% can be used.

The circuit is calibrated by using a known capacitance within the overall measurement range. Position 6 of the range switch places a 5% 0.005-μF polystyrene capacitor in the measurement loop. The 10-kilohm potentiometer then can be adjusted until the meter shows an exact half-scale (0.5-milliampere) reading.

Resistance switching cuts tone oscillator jitter

by Barry M. Kaufman
Compath Co., Redwood City, Calif.

If the bit rate is high enough for the bit period to approach or even become less than the tone signal period, 20% to 40% jitter distortion can be encountered when asynchronous digital data is transmitted with frequency-shift-keyed modems. A frequency-shift tone oscillator that delivers a phase-continuous, constant-amplitude signal significantly reduces this error.

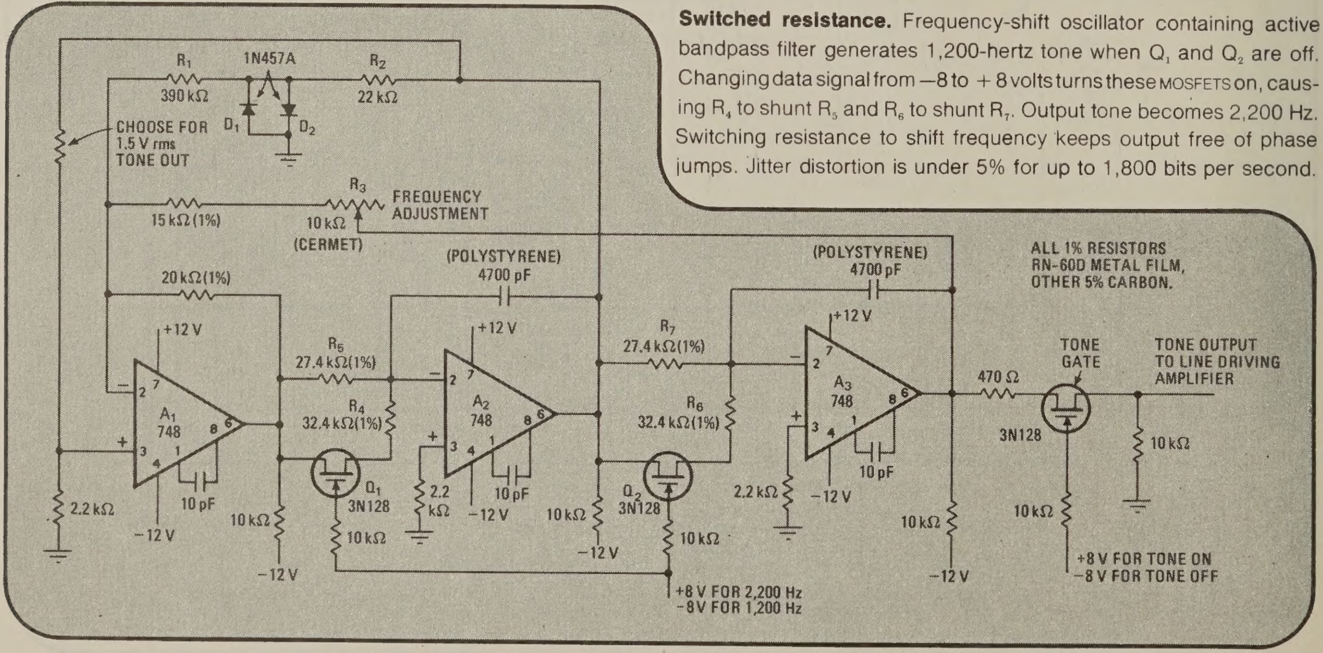
The tone oscillator holds jitter distortion to less than 5% at a data rate of 1,800 bits per second. The circuit employs a state-variable active bandpass filter that changes its frequency when resistance is switched.

Since switching resistance does not cause phase jumps, phase changes occur only at the incoming data signal transitions. The oscillator resonates at the filter frequency, generating a sine wave whose amplitude is limited by an anti-parallel diode pair.

Many conventional tone oscillators use an LC tank circuit as the resonating element so that a reactance must be switched to change the oscillator frequency. Jitter distortion can become significant because switching stored reactance energy not only generates phase jumps but also modulates signal amplitude. Furthermore, other oscillators frequently contain a square-wave multivibrator whose zero crossings seldom coincide with the zero crossings of the incoming asynchronous data.

The state-variable active bandpass filter in the low-jitter tone oscillator is formed by inverting amplifier A_1 and integrators A_2 and A_3. With positive feedback through resistors R_1 and R_2, the circuit oscillates at the filter frequency, which can be fine-tuned with R_3.

Because of its high Q, the active filter generates a



Switched resistance. Frequency-shift oscillator containing active bandpass filter generates 1,200-hertz tone when Q_1 and Q_2 are off. Changing data signal from −8 to +8 volts turns these MOSFETs on, causing R_4 to shunt R_5 and R_6 to shunt R_7. Output tone becomes 2,200 Hz. Switching resistance to shift frequency keeps output free of phase jumps. Jitter distortion is under 5% for up to 1,800 bits per second.

stable sine wave with less than 1% harmonic distortion. Signal amplitude is limited by diodes D_1 and D_2. The output MOSFET is a tone gate that can be controlled by an associated modem's request-to-send circuit.

The oscillator supplies two tones, 1,200 and 2,200 hertz, which are compatible with the popular Bell type 202 modem. When the data voltage is −8 volts, MOSFETs Q_1 and Q_2 are cut off and the 1,200-Hz tone is generated. If the voltage is changed to +8 V, Q_1 and Q_2 conduct, shunting resistor R_4 across R_5 and resistor R_6 across R_7; the output is the 2,200-Hz tone.

Tone amplitude remains constant because the time constants of both integrators are changed equally. The rate at which the phase shifts is the only tone signal parameter affected by the incoming digital binary data.

Doubling the divisor yields odd-order counter

by Charles Gordon and Thomas Chau
General Dynamics, Electric Boat division, Groton, Conn.

A simple concept makes it possible to achieve an often-difficult result—an odd-order counter that will deliver an output pulse train with a symmetrical duty cycle, as long as the input is a symmetric square wave. Usually, digital logic frequency dividers that have an odd divisor produce an unsymmetrical square wave.

The frequency divider shown first doubles input signal frequency (f_i) and then divides the resulting pulse train by twice the desired divisor (D). The output frequency (f_o) becomes:

$$f_o = 2f_i/2D = f_i/D$$

If a divide-by-seven counter must be built, the only components required are two-thirds of a hex inverter package, a dual NAND gate, and an eight-bit parallel-in/serial-out shift register. The register and one of the inverters divide the doubled input pulse train by a factor of 14.

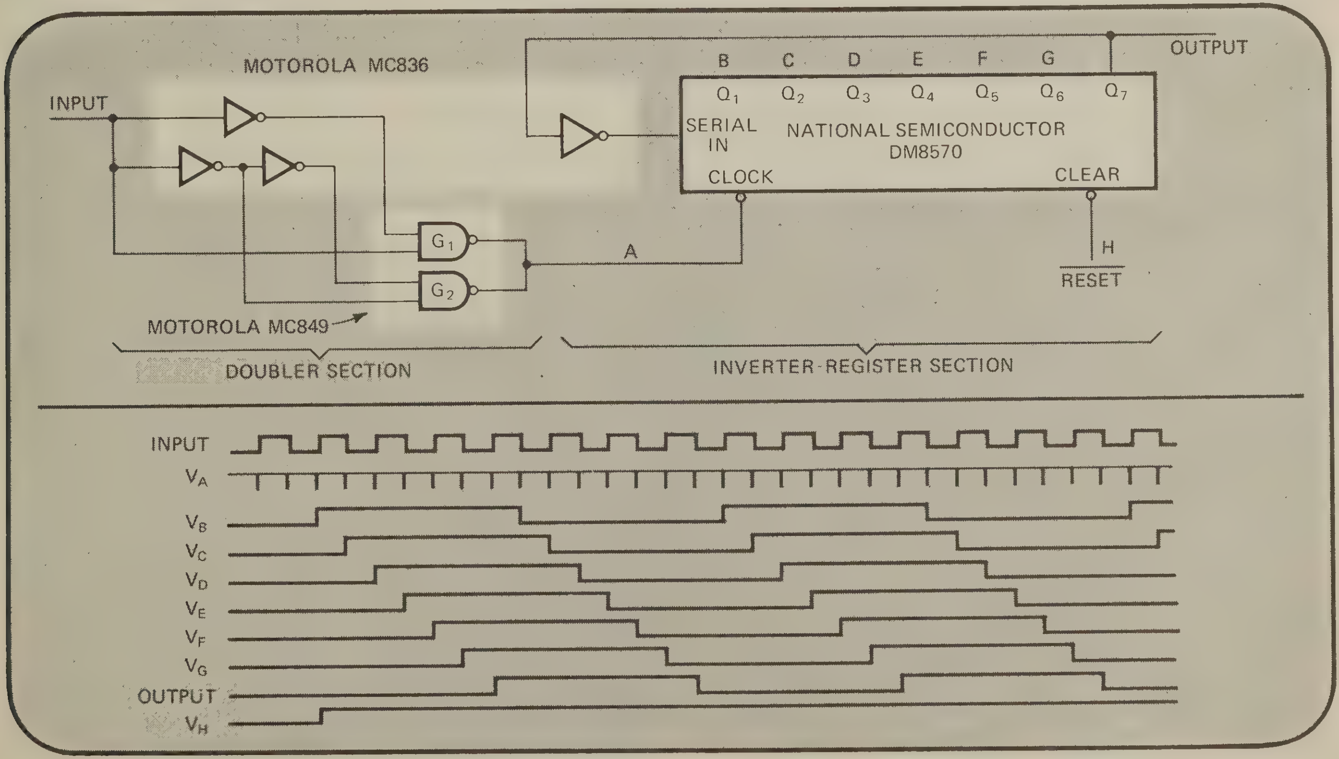
Three inverters and two NAND gates form the frequency doubler. The propagation delay of the logic elements themselves enables G_1 to contribute a pulse at each positive transition of the input, while G_2 contributes one at each negative transition. Since the outputs of the two gates are wire-ORed, the frequency of the input is doubled.

This $2f_i$ pulse train becomes the clock input for the shift register; it produces a single pulse for every eight clock pulses or one pulse for every seven of the input. The shift register must be reset initially.

If a divide-by-five counter is desired, the doubler section remains the same, but the output of the inverter-register section must be taken from the register's Q_5 terminal to divide the clock pulse by 10. To extend the divider scheme, additional shift registers must be used.

The propagation delays associated with the logic packages are not shown in the timing diagram.

Frequency divider. Odd-order symmetric counter can be implemented by doubling input frequency and then dividing by twice the desired divisor. Because of inverter propagation delays, G_1 is enabled at every positive input transition, G_2 at every negative transition, thus doubling input frequency. Inverter and register then divide doubled pulse train by 14 to realize divide-by-seven counter shown.



Divide-and-sample loop cuts phase-locked VCO slippage

by Charles Deming
Hughes Research Laboratories, Malibu, Calif.

A reference sine wave can be sampled to obtain the control voltage for a voltage-controlled oscillator (VCO) so that lock-in takes only about a dozen cycles. A steady intercycle voltage can be obtained for the VCO without the usual integrating circuit and its attendant delay—a common cause of initial instability.

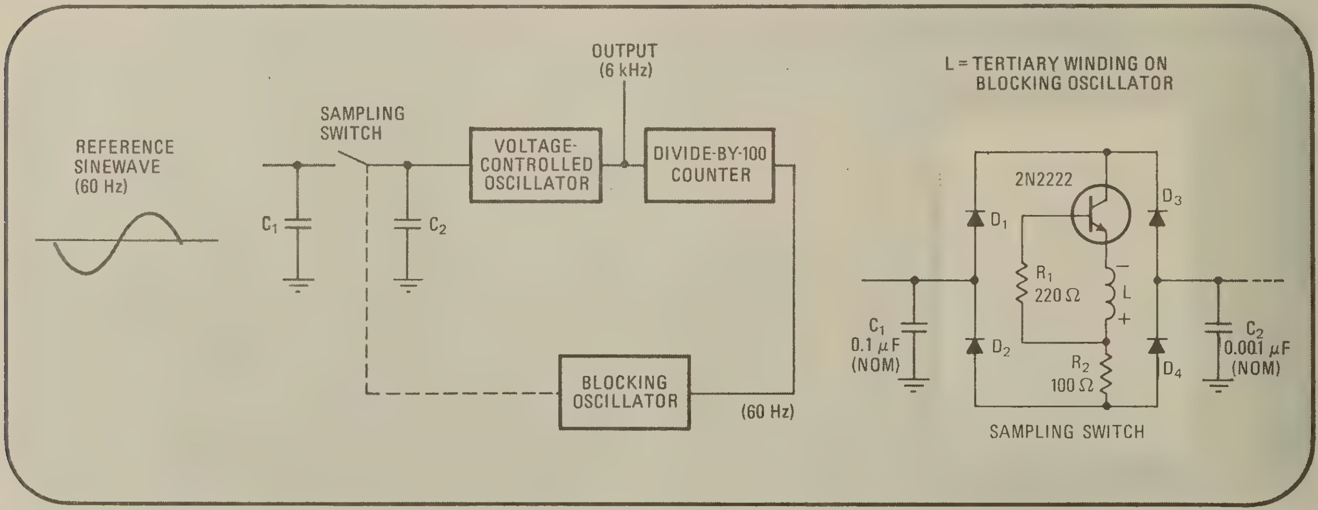
The reference frequency, 60 hertz in this case, appears across capacitor C_1. A sampling switch then transfers C_1's voltage at a given time to capacitor C_2. Sampling time must be short compared to the reference cycle time, and C_2 must be small compared to C_1. The sampled voltage controls the VCO.

Oscillator frequency is initially set to equal the reference frequency times the counter dividing factor. For this circuit, the VCO is set at 60 Hz (reference) times 100 (counter dividing factor) or 6 kilohertz. The counter, whose output is approximately 60 Hz, fires a blocking oscillator once per cycle to operate the sampling switch. The 6-kHz output frequency is now locked to the 60-Hz reference.

Except for its input and output connections, the sampling switch should be isolated from the circuit. The switch makes use of a tertiary winding on the blocking oscillator. In its off condition, the switch is open in both directions because a positive collector voltage is applied to the cutoff transistor. If C_1 is more negative than C_2, diodes D_1 and D_4 are back-biased; if C_1 is more positive than C_2, the back-biased diodes are D_2 and D_3.

During an on pulse, transistor base current is supplied by the tertiary winding and limited by resistor R_1. Transistor collector current is limited by resistor R_2 and flows through all diodes to close the switch. Although the transfer current between C_1 and C_2 is also limited, it can be made quite large because of its low duty cycle. The transfer of voltage, therefore, can be made quickly—within only a few microseconds for the 60-Hz oscillator.

Sine-wave reference. Phase-locked voltage-controlled oscillator employs 60-hertz reference to stabilize 6-kilohertz output. Reference sine wave is supplied across C_1. Switch then samples C_1's voltage and transfers it to C_2 for driving VCO. Blocking oscillator triggers sampling switch so that sampling phase difference prevents output frequency drift. Output frequency is reference frequency times counter factor.



Digital phase shifter maintains quadrature

by Kurt Leuenberger
Stanford Electronics Laboratories, Stanford, Calif.

When analog multipliers are used for phase detection, it is often necessary to maintain a 90° phase difference between the reference signal and the carrier of the modulated signal for optimum dynamic range and linearity. The carrier frequency, which is usually a known quantity that changes only by very small amounts, can be corrected for phase drift (from the desired 90° difference) with a digital phase-locked loop.

The digital phase shifter shown adjusts the reference phase for a zero dc output level so that a quadrature phase relationship can be maintained with the carrier of the incoming signal at frequency f_o. The unshifted reference signal must be available at the nth harmonic of f_o.

Two operational amplifiers, A_1 and A_2, perform as level detectors, sensing any excess dc level at the phase detector output. Detector A_1 supplies a logic 1 if its noninverting input is more positive than V_1; A_2 gives a logic 1 when its inverting input becomes more negative than $-V_1$.

When A_1 goes high, one-shot FF_1 (which consists of four NAND gates) is triggered by a positive output transition of gate G_1, corresponding to a positive transition of the reference signal. The one-shot then generates a pulse whose length, T_1, must be shorter than a half period of the reference signal.

This pulse enables gate G_3, and advances the counter. Therefore, the counter output signal at f_o is shifted to a leading position by 1/nth of a period.

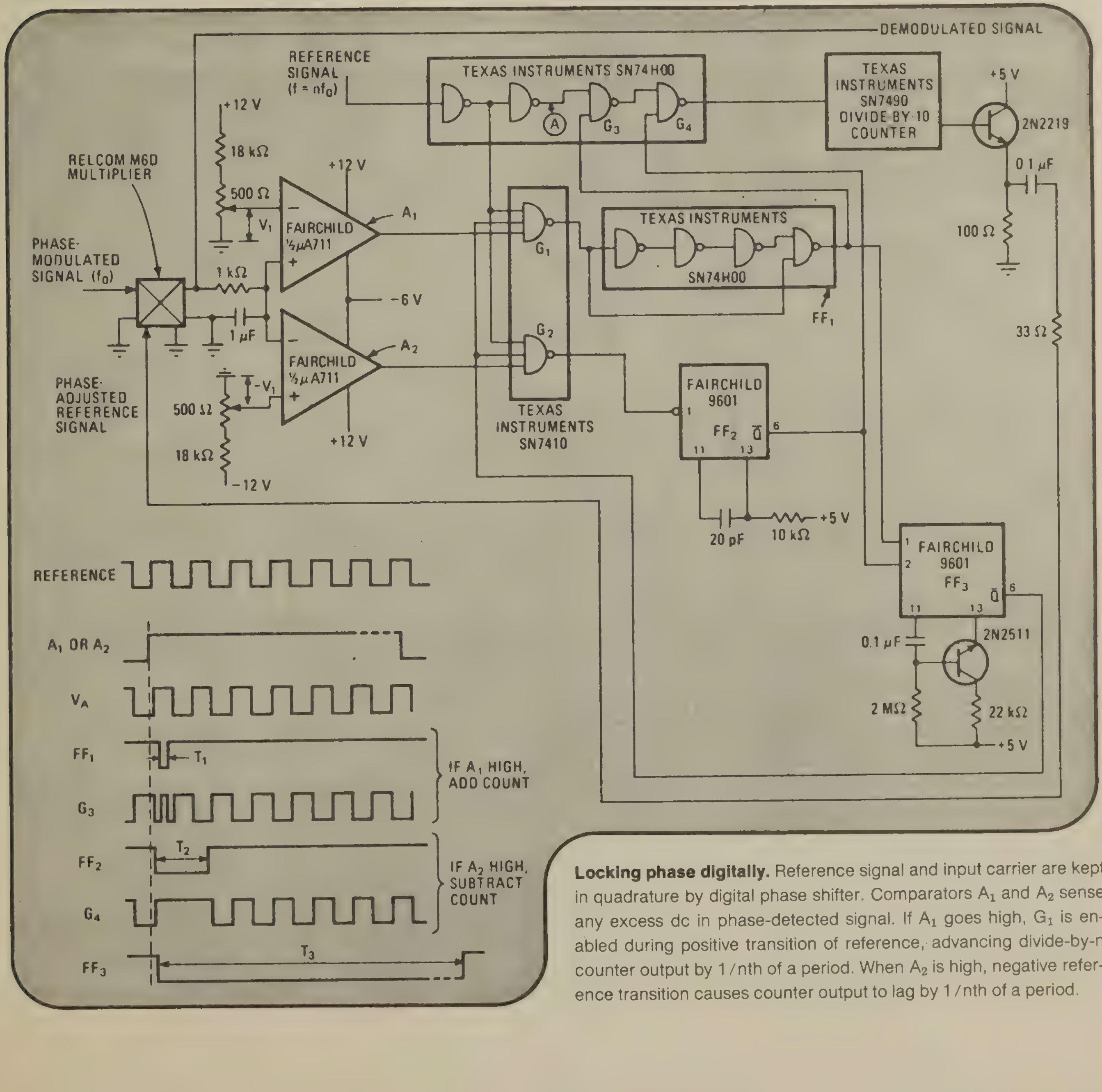
For negative reference-signal transitions, one-shot FF_2 is triggered by gate G_2, if A_2 is high. The one-shot's output is a pulse of length T_2 that enables G_4 and results in a suppressed positive transition at the counter input.

Phase shift now goes to a lagging position at the counter output by 1/nth of a period. Both FF_1 and FF_2 trigger one-shot FF_3, which inhibits the shift process at gates G_1 and G_2 for a time T_3, long enough for the entire loop to recover.

The circuit illustrated can be operated at a frequency (f_o) of 1 megahertz, with a dividing ratio (n) of 10 and inhibit timing (T_3) of 0.1 second. The error voltage to which the loop responds can be decreased by increasing the dividing ratio.

It is also possible to use the digital phase shifter as an open-loop circuit for phase or frequency modulation to tens of kilohertz. Modulation is accomplished by reducing T_3 and by keeping either A_1 or A_2 high to generate a continuous count addition or subtraction.

Output waveforms are shown for several points in the circuit.



Locking phase digitally. Reference signal and input carrier are kept in quadrature by digital phase shifter. Comparators A_1 and A_2 sense any excess dc in phase-detected signal. If A_1 goes high, G_1 is enabled during positive transition of reference, advancing divide-by-n counter output by 1/nth of a period. When A_2 is high, negative reference transition causes counter output to lag by 1/nth of a period.

Instrument amplifier offers high gain

by Richard S. Burwen
Analog Devices Inc., Norwood, Mass.

Intended for use as an input stage for dc laboratory instruments, an amplifier circuit provides a dc gain of 1 to 1,000, while maintaining a gain-bandwidth product of approximately 200 kilohertz. Amplifier gain is switch-selectable in decade steps.

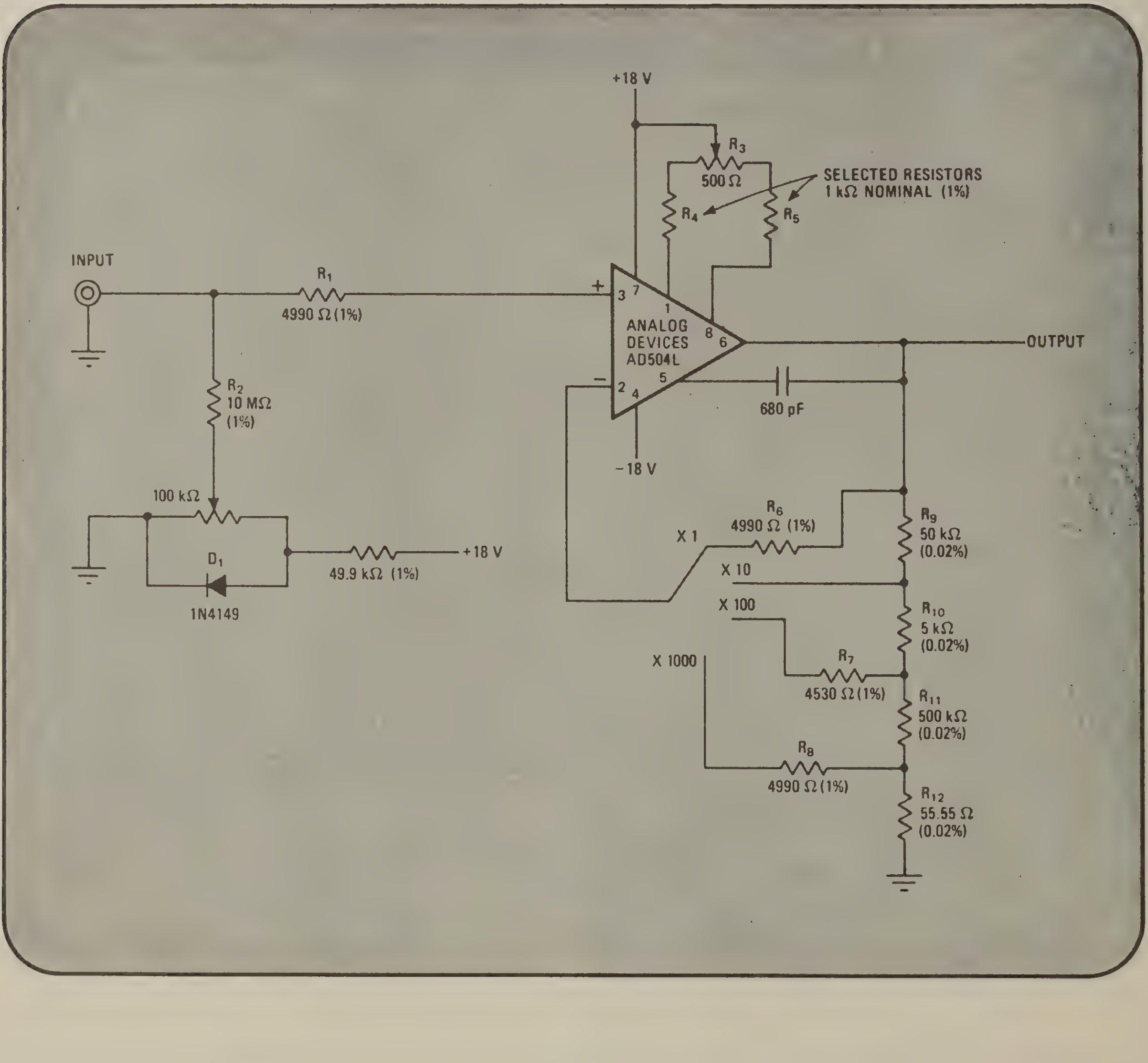
Series input resistor R_1 protects the amplifier against overvoltages of up to ±20 volts whenever the power supplies are turned off. Resistor R_2 determines the circuit input impedance (10 megohms in this case) and is used to zero amplifier input bias current by means of the temperature-compensating (due to diode characteristic) reference voltage developed across diode D_1.

Amplifier offset voltage is zeroed with potentiometer R_3. A pair of selected resistors (R_4 and R_5) reduces the voltage span of R_3 to about 400 microvolts, referred to the amplifier input. Selection of R_4 and R_5 is necessary to permit offset adjustment with R_3 since the amplifier has a rated offset voltage of ±0.5 millivolt. If a coarser adjustment can be tolerated, a single 10-kilohm pot can replace R_3, R_4, and R_5.

A feedback network, consisting of resistors R_6 through R_{12}, allows amplifier gain to be switched in decade steps. This network also provides a constant source impedance for the amplifier's inverting input. Because of resistor arrangement, circuit output is zeroed (with no input applied) for all gain ranges if it is zeroed for the highest one.

The circuit can attain overranging of ±150%.

Instrument aid. Reference voltage for instrument input amplifier is developed with diode D_1, compensating for amplifier input bias current through 100-kilohm pot and resistor R_2. Offset zeroing is accomplished with potentiometer R_3 and resistors R_4 and R_5. Feedback resistor network permits gain selection from 1 to 1,000. Impedance at amplifier inverting input remains constant, no matter where switch is set.



Interrupt register secures all data signals

by D.J. Plummer and T.E. Zinneman
Indiana University, Bloomington, Ind.

A real-time computer frequently must respond to signals produced by such devices as counters and timers. If a latching interrupt register is used for detection, register dead time can be eliminated so that valuable data signals are not lost.

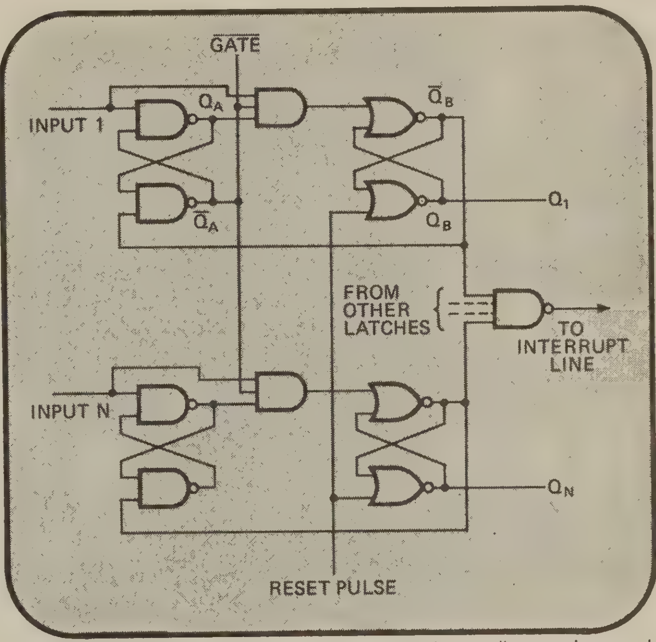
Normally, an interrupt register consisting of several flip-flops is used. The outputs of the flip-flops are wire-ORed together onto one interrupt line. When it receives an interrupt signal, the computer reads the interrupt register to determine what device requires service. The register then is reset to remove the signal from the interrupt line.

However, if a signal occurs on another input line during the reading and resetting of the register, it is highly probable that the computer will not detect the signal. Although this "dead time" may only be several microseconds, important device interrupt signals can be lost.

The interrupt register shown overcomes this difficulty. Basically, it accommodates N inputs, and consists of a NAND gate latch, an AND gate, and a NOR gate latch. For a logic 0 input, the NAND latch is set ($Q_A = 1$), and the NOR latch is reset ($Q_B = 0$). When an input goes high, the level transition enables the AND gate, setting the NOR latch ($Q_B = 1$). This triggers the interrupt line and resets the NAND latch ($Q_A = 0$) to prevent the interrupt line from being triggered by the same signal.

The gate signal, which is normally high, only goes low during the reading-and-resetting sequence, an operation that takes only a few microseconds. When the gate signal is low, all NOR latches are isolated from the inputs and cannot be set by incoming signals. As soon as the gate goes high, a new input signal sets the NOR latch.

To avoid missing any interrupts, the duration of an input signal must be longer than the time the gate signal is low. The gate and reset signals may be obtained from one-shots that are triggered by a strobe signal, which is generated when the computer is ready to read the register.



Safeguarding multiple data. Interrupt register allows wire-ORed data signals to be gathered by computer, while register is being read or reset. NAND latch is initially set. Input signal enables AND gate and sets NOR latch; this triggers interrupt line for computer readout and resets NAND latch. All inputs are read as long as time that gate signal is low is shorter than duration of input signal.

Voltage-frequency converter uses four-layer diode

by T.C. O'Haver
University of Maryland, College Park, Md.

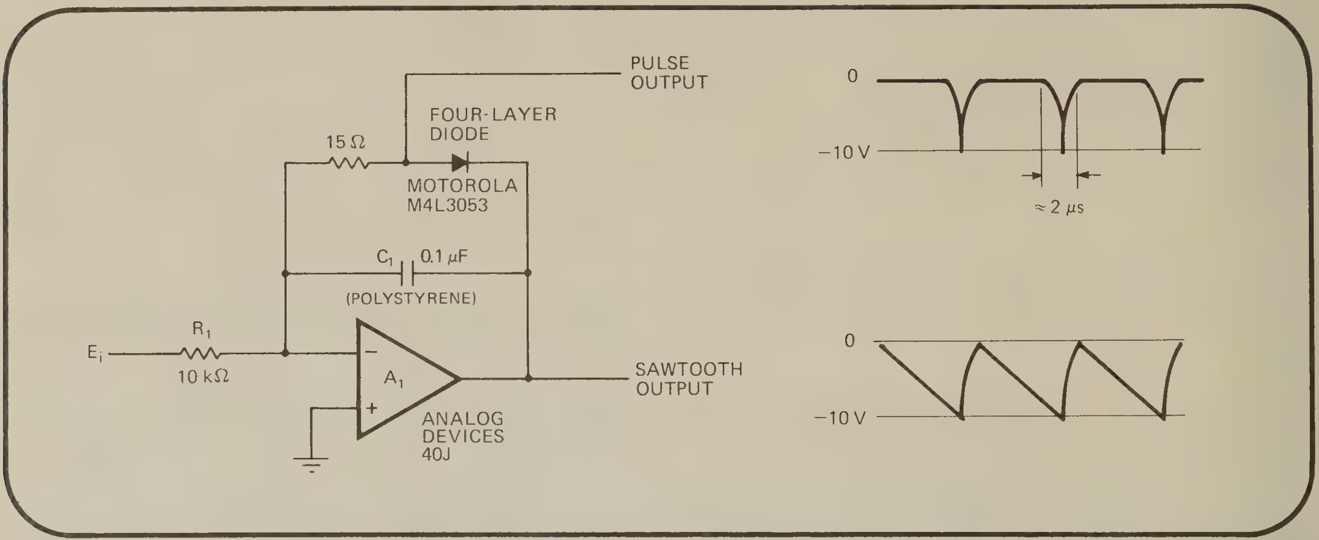
By using a four-layer diode to reset a conventional dc integrator to a fixed potential, a voltage-to-frequency converter (or voltage-controlled oscillator) can be built with only one operational amplifier and four other components. The circuit offers a conversion linearity of better than ±0.2% of full scale from 0 to 10 volts. In addition, both sawtooth and pulse outputs are available.

The dc input voltage is integrated by amplifier A_1, resistor R_1, and capacitor C_1, producing a ramp with a slope of $-E_i/R_1C_1$ volts per second. When this output sawtooth exceeds the forward threshold voltage (E_t) of the four-layer diode, the diode switches into its low-impedance stage.

Capacitor C_1 now discharges until the voltage across it is approximately 1 v (diode recovery voltage). The diode then recovers and the cycle repeats. Because of the switching action of the diode, a pulse output is also produced at the diode's anode terminal. The frequency of the output sawtooth is about $E_i/R_1C_1(E_t - 1)$.

Any general-purpose operational amplifier will perform satisfactorily; total parts cost is about \$6 to \$20. For the components shown, output frequency is about 100 hertz per volt, with a linearity of ±0.2% of full scale for inputs from 0 to 10 V and less than ±0.2% of reading from 0.2 to 2 V. Similar results can be obtained with capacitor values of 0.01 to 1 microfarad.

Better linearity can be obtained by using a 1-^{m}F capacitor, but at the expense of reduced output frequency. The circuit operates well up to 5 kilohertz; however, it becomes limited at higher frequencies by op amp slew rate. The value of R_1 should be chosen to keep amplifier input current above 10 microamperes to avoid errors due to diode leakage current.



Switching integrator. Four-layer diode serves as voltage comparator and reset switch for voltage-to-frequency converter. A_1, R_1, and C_1 produce sawtooth output by integrating dc input. When output ramp reaches diode threshold voltage, the diode conducts and discharges C_1. Cycle repeats when capacitor voltage drops to diode recovery voltage. Pulse output is due to voltage drop across 15-ohm resistor.

IC transistor array compensates for temperature

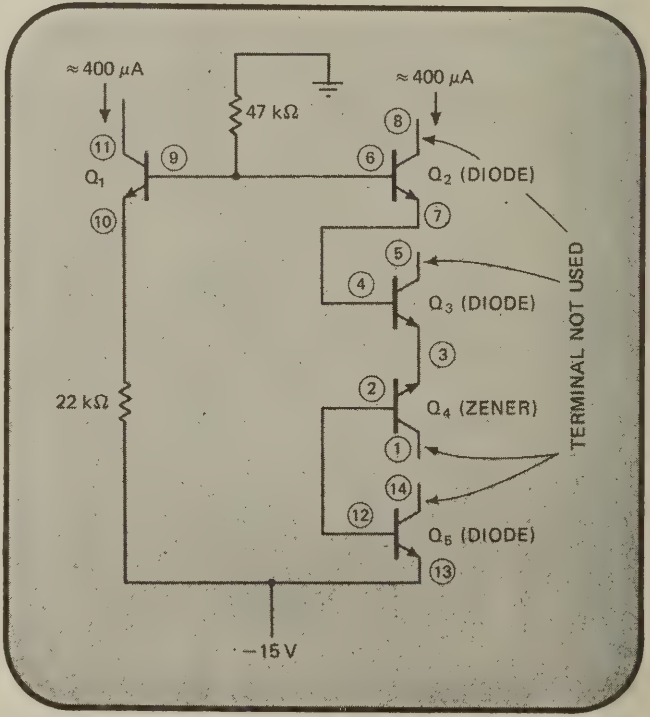
by Arthur Chace
Mount Holyoke College, South Hadley, Mass.

An inexpensive integrated transistor circuit can supply a constant current while providing its own temperature compensation. This combination of characteristics is especially useful when a differential FET-input amplifier has to be biased at its zero-temperature-coefficient point [*Electronics,* June 21, p. 76], because the amplifier's constant-current source should be temperature-compensated for optimum performance.

All five transistors in RCA's type CA3046 package are used. Transistor Q_1 operates as a conventional transistor, but the other four are employed as diodes—Q_2, Q_3 and Q_5 as forward-biased diodes, and Q_4 as a zener diode.

The temperature coefficient of diode element Q_2 matches that of transistor Q_1. And the positive temperature coefficient of the zener element is compensated for by the identical, but negative, coefficients of Q_3 and Q_5. Since all circuit elements are on a common substrate, temperature tracking of individual elements is good.

The emitter of Q_5 is connected to the substrate and should be the most negative point in the circuit.



Compensating a FET amplifier. Five-transistor integrated circuit array can be used as temperature-compensated constant-current source for FET-input differential amplifier. Q_1 operates as a conventional transistor; elements Q_2 through Q_5 are diodes. Q_2 compensates Q_1, while Q_3 and Q_5 compensate zener element Q_4. IC package pin numbers are indicated by circled numbers.

A-d converter provides real-time error correction

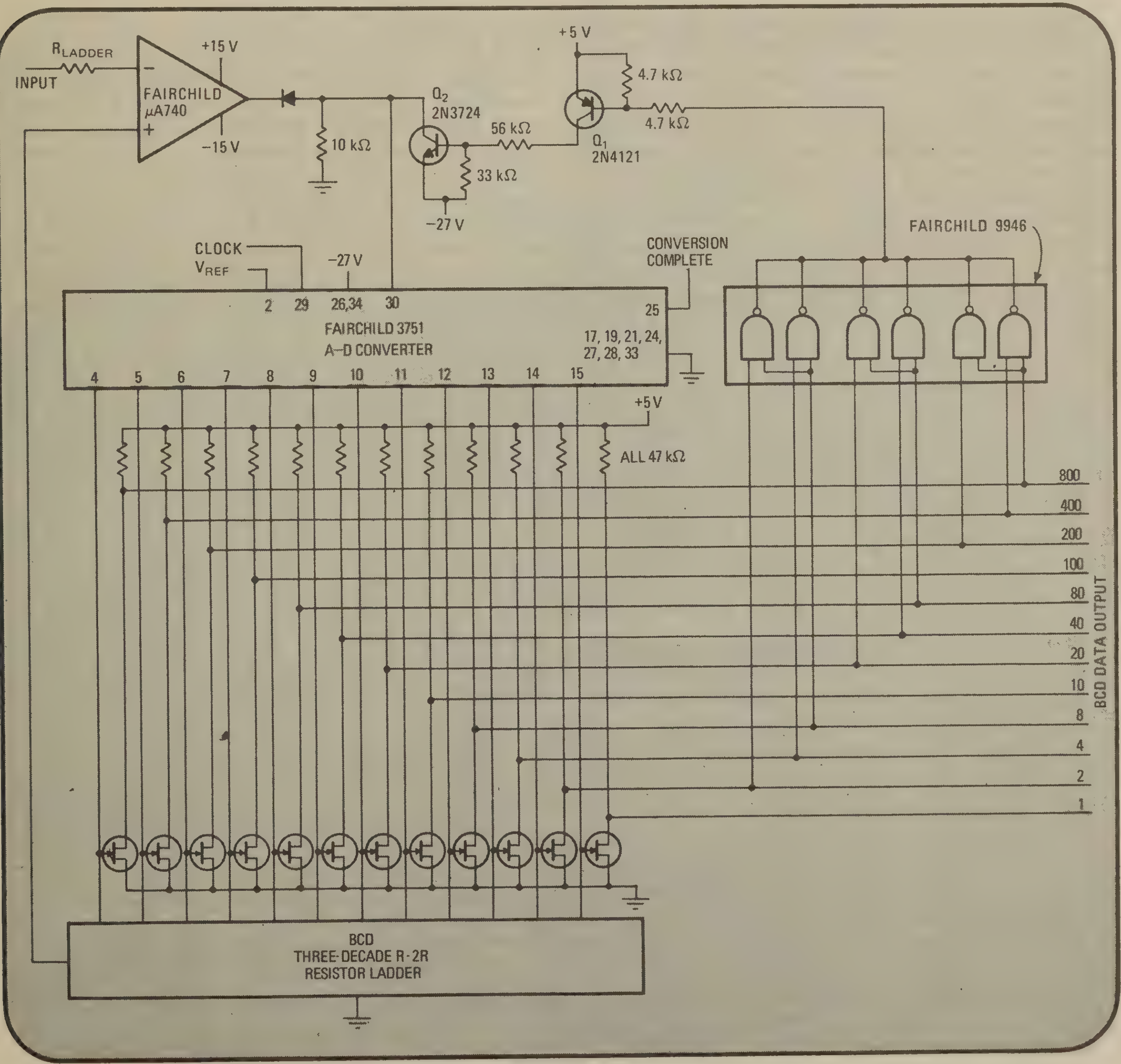
by Marvin K. Vander Kooi*
National Semiconductor Corp., Santa Clara, Calif.

By adding comparator logic to an analog-to-digital converter, the latter can be stopped from producing an "illegal" output code due to noise pulses or voltage drift.

Whenever a converter with a binary-coded-decimal (BCD) output operates on a signal having adjacent digit 9s, a code error may result. If the last 9 contains a noise pulse equal to only 0.001 of the full-scale signal, the BCD output may become 10-0. The "illegal" 10 cannot be handled by a BCD input to a computer, nor can it be displayed as a single digit on a readout device. With a successive-approximation a-d converter, these "illegal" codes can be detected since the converter is always comparing its output to its input.

In brief, the converter's output is detected by the NAND gates and changed to negative-voltage logic by Q_1 and Q_2. When Q_2 conducts, it overrides the comparator output, causing the converter to reject the "illegal" bit. On the next clock pulse, the converter moves to the next bit.

BCD code correction. "Illegal" BCD output codes caused by noise or drift are detected by NAND gates and converted to negative-voltage logic. When transistors Q_1 and Q_2 conduct, they override comparator output, preventing analog-to-digital converter from accepting "illegal" bit. An "illegal" bit, a 10, usually occurs when signal containing a 9 also carries small unwanted noise or drift voltage.



---

*Formerly with Fairchild Semiconductor, Mountain View, Calif.

Low-voltage regulator uses reversed error amplifier

by Claus H. Claasen
IBM Corp., Systems Development division, San Jose, Calif.

A regulator circuit with an upside-down error amplifier can provide a regulated voltage of less than 4 volts at 2 amperes, while operating from a higher-voltage unregulated supply. Since zener diodes and IC regulators cannot supply an output at this voltage and current level, an auxiliary voltage of opposite polarity is commonly used to achieve low-voltage regulation. The voltage may be obtained from another supply or from an existing circuit voltage.

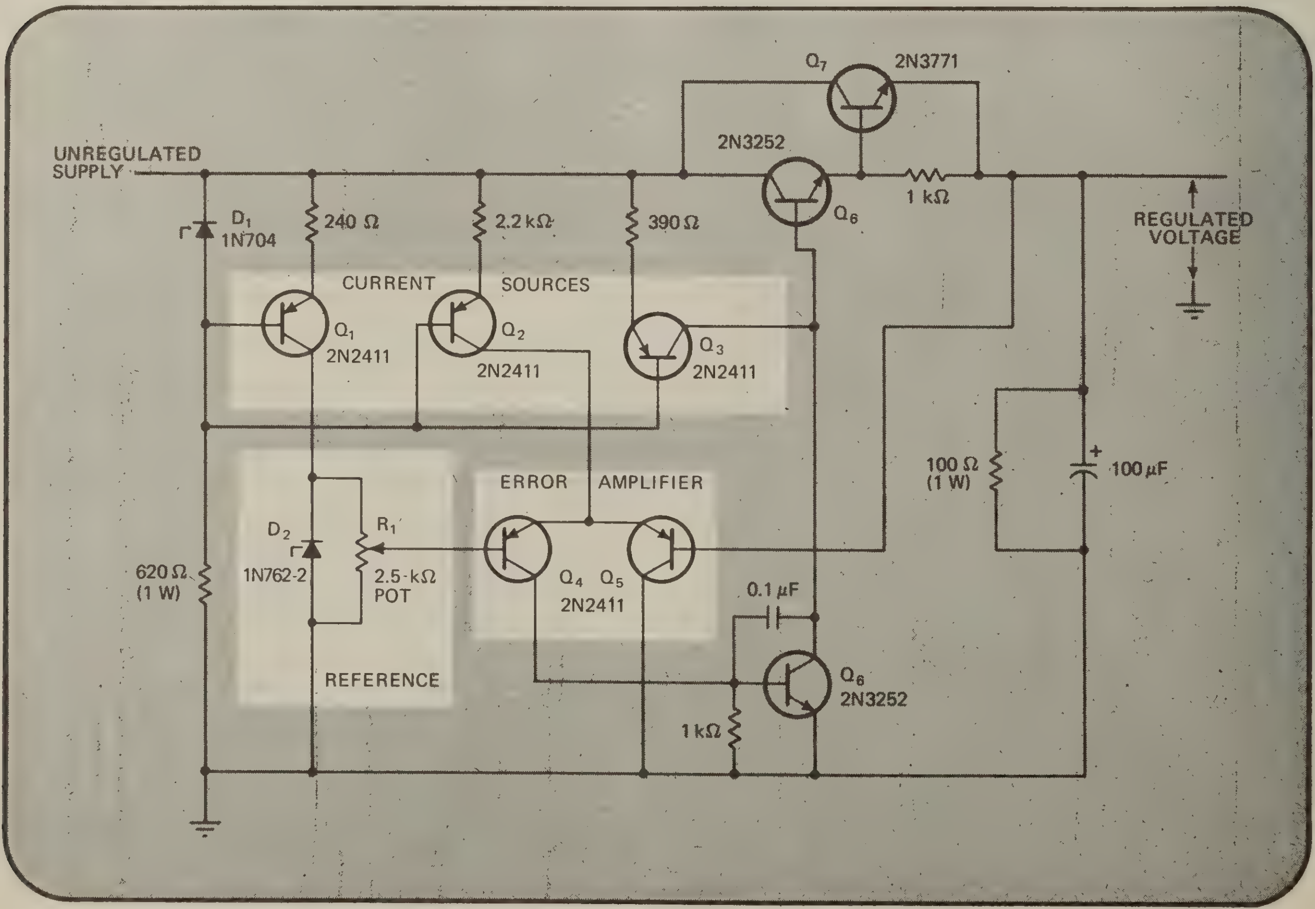
Reversing the regulator's error amplifier and inverting the amplifier's output with a current-sink transistor can result in voltages of less than 1 V and a regulation of better than 1%. The circuit shown provides a low positive voltage, but a small negative output can be obtained very simply if all diodes are reversed and all npn transistors changed to pnp types and vice-versa.

Zener diode D_1 is a common reference for current sources Q_1, Q_2, and Q_3. Transistor Q_1 feeds zener voltage reference D_2; Q_2 supplies the error amplifier, which consists of transistors Q_4 and Q_5; and Q_3 feeds a series pass element, the Darlington configuration of Q_6 and Q_7.

Under the control of the error amplifier, transistor Q_8 sinks all or part of the current coming from Q_3. The error amplifier compares the regulated voltage with a fraction of the reference voltage, as determined by potentiometer R_1.

For the components indicated, the circuit regulates 3.2 V at 2 A maximum from an unregulated supply of 14 V nominal. When unregulated supply tolerance is ±10%, circuit regulation is better than ±1% after initial adjustment. A regulated output of 1 V can be obtained from an unregulated supply of about 8 V.

Regulating small voltages. Regulator circuit supplies output voltages as low as 1 V. Current sources Q_1, Q_2, and Q_3 feed zener reference (D_2 and R_1), error amplifier (Q_4 and Q_5), and series-pass Darlington pair (Q_6 and Q_7), respectively. Error amplifier compares regulated output to zener reference, while Q_8 acts as current sink for Q_3. Circuit provides 3.2-V regulated voltage from 14-V bulk supply.



Hard-limited sinusoid eases frequency multiplication

by Donald F. Dekold
University of Florida, Gainesville, Fla.

An audio-frequency multiplier achieves a multiplication factor of 40 (for a 625-hertz input) by hard-limiting a damped sine wave. The design uses a minimum of components and circumvents the problem of inherently low-Q inductors at audio frequencies.

If the input is a symmetrical square wave, the circuit performs odd multiplication; for an asymmetrical square wave, it functions as an even multiplier. A true square wave can only yield odd harmonics, but even harmonics can be introduced by varying the square wave's duty cycle. For even or odd multiplication, both tank circuits will ring at their natural frequency.

Due to L_1's normally low Q, the ringing response will be a damped sinusoid (e_a). Resistor R_1 isolates the tank circuit from a source that may have a low output impedance, which could further lower the tank's Q. Since the field effect transistor has nearly infinite input impedance, it does not load the tank circuit.

Because the input is periodic with a frequency of f_o, the ringing responses are also periodic. A source-follower stage couples these periodic ringing waveforms into an integrated circuit limiter.

Due to the high gain of the limiter, the ringing waveform is hard-limited, and the decaying sinusoid becomes a positive quasi-square wave of relatively constant amplitude at point b. The voltage, e_b, appears across load resistor R_2.

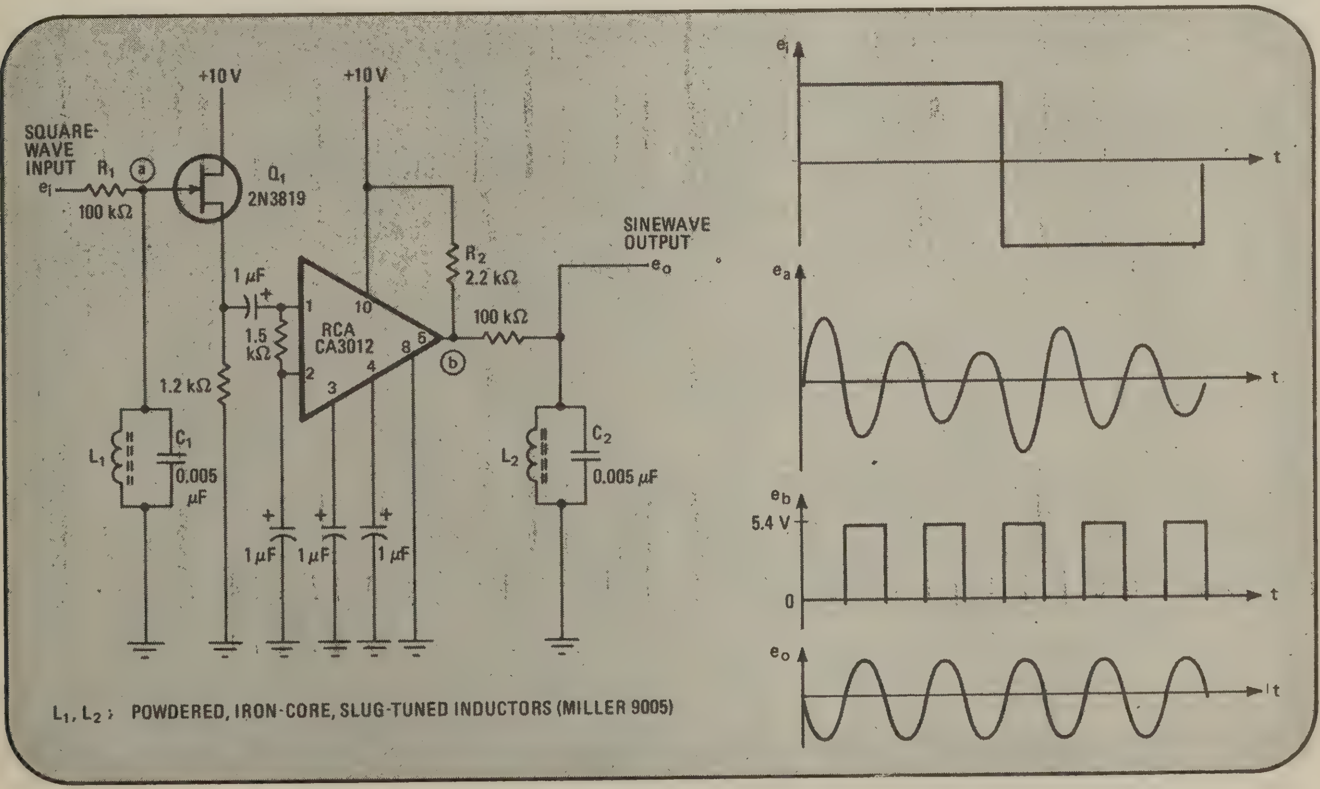
Another tuned circuit, formed by L_2 and C_2, filters the limiter's output, producing a sine wave whose frequency is nf_o. The filtering task at this point in the circuit is easy, since the limiter's constant-amplitude output primarily contains frequency component nf_o and odd multiples of nf_o. The single tank circuit is sufficient to provide sine waves with good spectral purity.

Care must be taken to adjust both tuned circuits so that their natural (ringing) frequencies are exactly the desired multiples of the input frequency. If this is not done precisely, an objectionable amount of spectral impurity appears in the output signal as amplitude modulation.

For an input frequency of 625 Hz, the multiplier produces an output frequency of 25 kilohertz, which corresponds to a period of 40 microseconds. The total period of the input square wave is, of course, 40 times the period of the output sine wave.

In addition, the duty cycle of the input square wave must be adjusted so that it can be coupled into the first tank with a phase relationship that does not destructively interfere with the tank's ringing voltage. An asymmetrical square wave of this type can be supplied by a one-shot multivibrator. For example, a standard one-shot with a variable pulse-width control can be used as the multiplier's input stage; the one-shot would be driven by a source whose frequency is f_o. The waveforms shown are for a times-five multiplier.

Multiplying audio frequencies. Either symmetrical or asymmetrical input square wave causes L_1C_1 tank circuit to ring at its natural frequency; symmetrical square waves yield odd multiplication, asymmetrical yield even. Source-follower couples ringing waveform into wide-range limiter. Resulting pulse train is filtered by second tank (L_2C_2), producing sine wave. Multiplication factor is 40 for 625-hertz input.



L₁, L₂ : POWDERED, IRON-CORE, SLUG-TUNED INDUCTORS (MILLER 9005)

Flip-flop sequences conversion register

by Richard J. Mann
TRW Systems, Redondo Beach, Calif.

The conversion register for a successive-approximation analog-to-digital converter can be made to sequence automatically by adding a control flip-flop. Usually, bit time signals are used to sequence cell setting and conditional resetting in the conversion register.

If the converter is closely associated with a large digital system, these bit time signals generally are available. But if the converter is a remote self-contained unit, a counter and a decoder must be added to generate the bit-time signals. A more efficient register design eliminates this extra circuitry by adding one flip-flop.

If the register is seen as a conventional sequential machine, its operation can be represented by a state map, as illustrated in (a) for four-bit conversion. The conversion sequence begins with the most-significant bit, the 1000–0 state, which corresponds to the midscale analog value.

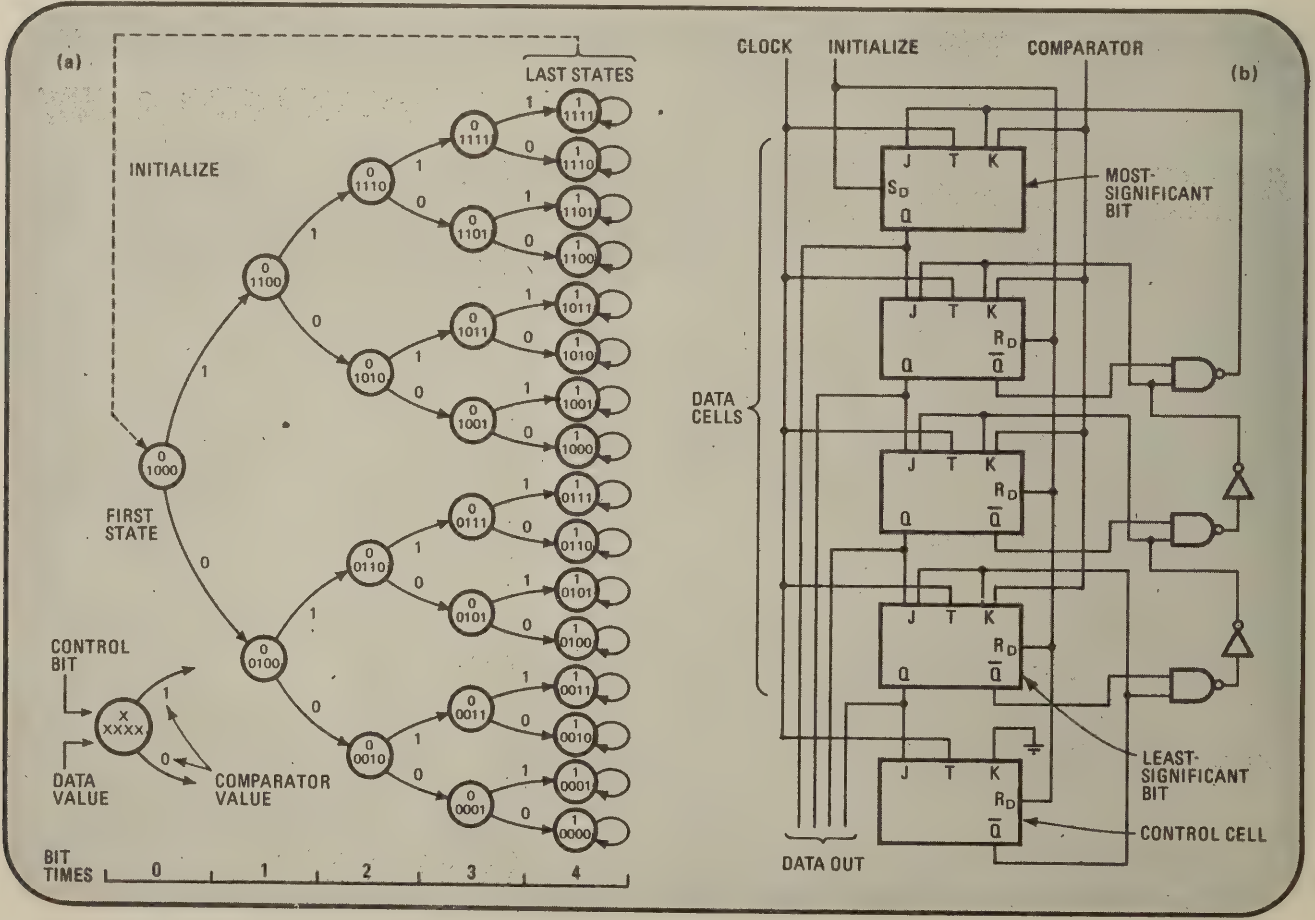
After a comparison between this analog value and the data value, the first cell may or may not be reset. In either case, the next cell is set. For example, the register will jump from the 1000–0 state to the 1100–0 or the 0100–0 state depending on the comparator value. This process is repeated for each less-significant bit.

Therefore, the register for an n-bit converter is sequenced from its initial 1000–0 state to one of 2^n possible final states. Since the total number of register states is $2^{n+1} - 1$, adding a flip-flop as a control bit permits each register state to have a unique value so that the register is self-controlled.

The last state always has a logic 1 as the control bit. Depending on system requirements, a 1 in the control cell permits the control bit to signal completion of a conversion cycle, to dump the register data into an external buffer, to make the converter wait for data sampling by the user, or to initiate a new conversion cycle. In any case, re-initialization occurs by forcing the 1000–0 state and clearing the control bit.

An auto-sequencing four-bit register, then, can be implemented with five flip-flops (b). The mechanization scheme, which is easily expandable to any number of bits, uses J-K flip-flops like Texas Instruments' type SN5472. Converter operation is stop-and-hold.

Automatic sequencing. State map of register (a) for four-bit a-d converter shows $2^5 - 1$ total states, and $2^4 - 1$ final states, indicating that self-sequenced operation can be realized with extra flip-flop. Self-controlled four-bit register (b) uses five flip-flops, instead of usual four. In general, n-bit converter has 2^n final states, $2^{n+1} - 1$ total states, and requires n + 1 flip-flops for automatic sequencing.



Comparator logic limits switching regulator current

by Robert S. Olla
National Semiconductor Corp., Sunnyvale, Calif.

A switching regulator that uses digital current limiting provides a current regulation of better than 1%, while offering good frequency stability and fast response to transients. Essentially, the regulator uses two NAND gates as a pulse-width modulator to keep current from exceeding the present limit.

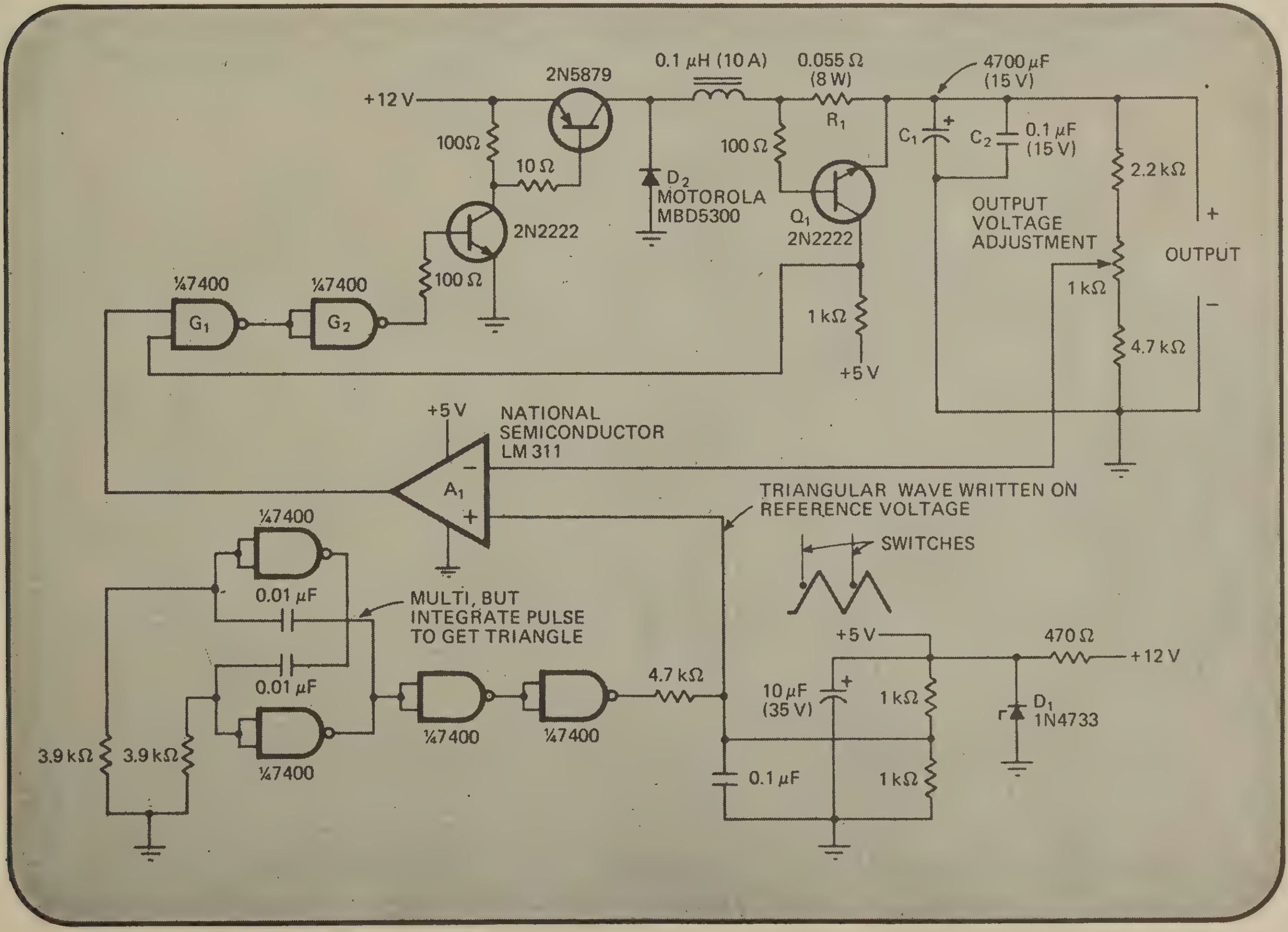
The circuit employs a zener diode, D_1, to provide both the circuit reference voltage and supply power for the logic. A hot-carrier diode, D_2, is used for efficient elimination of spikes in the output.

As long as the current limit, I_L, is not exceeded, transistor Q_1 remains off; I_L is determined by the value of resistor R_1. For the resistor shown, I_L approximately equals 10 amperes.

The signal at Q_1's collector is used to inhibit the output pulses from comparator A_1. When Q_1 is off, all pulses pass through NAND gates G_1 and G_2. However, if I_L exceeds the preset 10 A, Q_1 conducts, and its collector voltage goes low. This inhibits the comparator pulses until the current falls below I_L.

A triangular wave is applied to the noninverting comparator input. It is obtained from a multivibrator whose pulse output is integrated and written on the zener reference voltage. The comparator switches one time during each triangle cycle, when the wave's slope is positive; the switching point is determined by setting the 1-kilohm potentiometer. Operating frequency of the switching regulator is the frequency of the triangular wave.

Digital current limiting. Output current of switching regulator is held to desired limit by digital comparator. Transistor Q_1 remains off as long as current limit is not exceeded. If current goes beyond limit, Q_1 turns on, inhibiting A_1's output pulses. NAND gates G_1 and G_2 form pulse-width modulator; zener diode D_1 supplies regulator's reference voltage. Current limit for circuit shown is 10 amperes.



Transistor matrix driver supplies varying loads

by S.S. Durvasula
Honeywell Information Systems, Framingham, Mass.

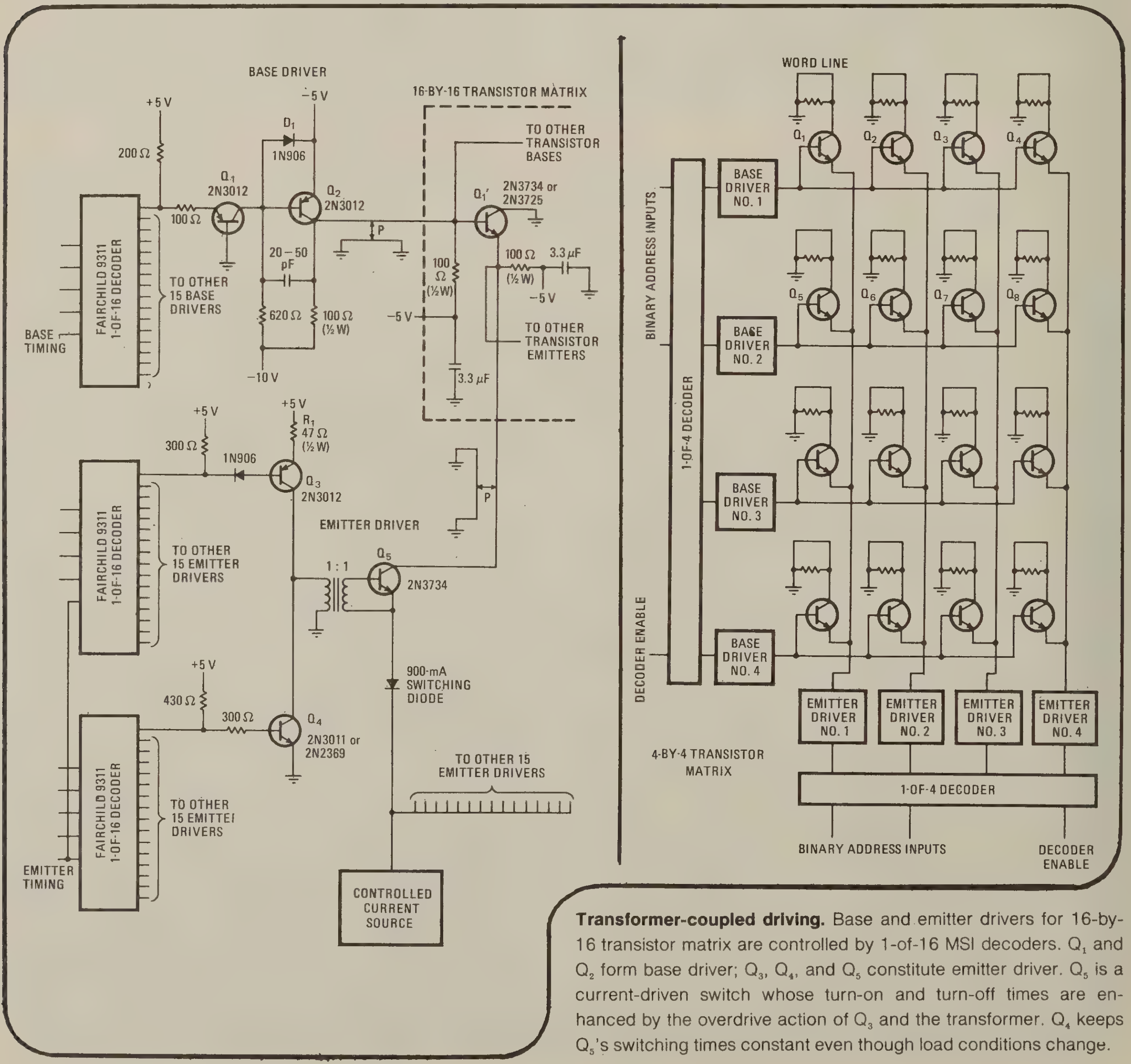
Testing magnetic memory planes containing transistor matrices often requires special drive circuitry between the decoding logic and matrix because of varying signal conditions. The matrix drive circuitry illustrated compensates for these changing signal and load variations, and yet maintains power dissipation at a minimum. The decoding logic used in the matrix driver circuitry is greatly simplified by the use of medium-scale integrated circuits, like three 1-of-16 decoders.

There are 16 base and 16 emitter circuits to drive the 16-by-16 transistor matrix. Operating the matrix may require switching pulses of up to 900 milliamperes with 40-nanosecond rise and fall times. This should be provided by a current source that controls pulse amplitude and width, and maintains specific pulse rise and fall times.

Operation of the matrix base drive is straightforward. When the top decoder's output is high, Q_1 is on, and Q_2 is off since D_1 clamps the base of Q_2 at a diode drop above –5 volts. Once the decoder goes low, Q_1 turns off and Q_2 saturates, driving the base bus of Q_1 through a twisted pair.

Emitter drive operation is slightly more complex. Normally, the decoder outputs that feed Q_3 and Q_4 are high, keeping Q_4 on, and Q_3 and Q_5 off. When the decoder outputs go low, Q_3 turns on, Q_4 turns off, allowing Q_5, which is a current-driven switch whose base drive is fixed by R_1, to conduct. Current flows through Q_4's collector-emitter junction only when the decoder control voltage is changing.

The load requirements of Q_5 are for controlled cur-



Transformer-coupled driving. Base and emitter drivers for 16-by-16 transistor matrix are controlled by 1-of-16 MSI decoders. Q_1 and Q_2 form base driver; Q_3, Q_4, and Q_5 constitute emitter driver. Q_5 is a current-driven switch whose turn-on and turn-off times are enhanced by the overdrive action of Q_3 and the transformer. Q_4 keeps Q_5's switching times constant even though load conditions change.

rent and pulse conditions. But since the voltage excursions of Q_5's collector and emitter could vary over a wide range, a transformer-coupled drive is used to correct for changing load conditions.

Transistor Q_3 and the transformer provide overdrive for a pulse leading edge so that Q_5 turns on quickly. When current flows in the opposite direction during a pulse trailing edge, transformer droop removes any stored charge from the base of Q_5, forcing it to turn off quickly.

Since the circuit must accommodate varying pulse widths, Q_4 is used to make Q_5's turn-on and turn-off times always as fast as possible. Although the leading-edge overdrive, which is fixed by R_1, is not affected by narrow pulse widths, transformer droop is no longer available to enhance turn-off time. However, during the trailing edge of a narrow pulse, Q_4 turns on and provides a reverse current through the transformer droop and decreasing Q_5's turn-off time.

Matrix bases and emitters not selected look like capacitances distributed along the bus lines. The capacitance per transistor depends on the back-bias voltage at the base-emitter junction of the unselected device; it can be determined from manufacturer's specifications.

FET current source gives stable, precise ramp

by Thomas D. Price
Saunderstown, R.I.

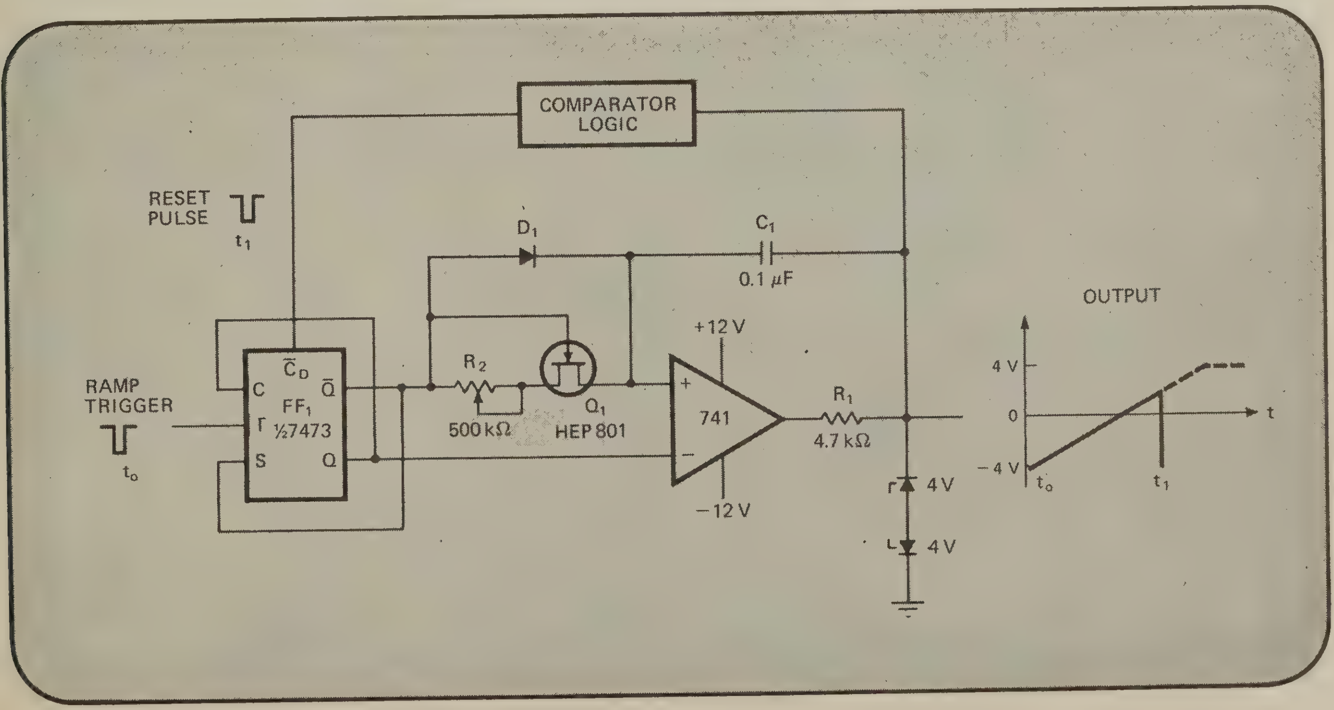
Employing a field effect transistor as a constant-current source in a ramp generator can produce an output with a linearity and slope that is virtually independent of unwanted variations in control voltages. The resulting circuit is a stable, highly linear ramp generator that is both simple and inexpensive to build.

Before the ramp trigger is applied, the Q output of flip-flop FF_1 is low and the amplifier output is clamped low by back-to-back zener diodes. Resistor R_1 limits amplifier short-circuit current. At time t_0, the ramp trigger causes the Q output of FF_1 to go high, producing an output ramp whose rate is determined by the value of capacitor C_1, and a constant current from FET Q_1, which is set by resistor R_2. (For this circuit, ramp slope is 100 volts per second.)

The output ramp, in turn, drives external comparator logic, which produces a reset pulse for FF_1 at time t_1. The pulse input at t_1 is preset at some desired voltage level: for instance, an unknown voltage that is being measured. Once FF_1 is reset, its Q output goes high, C_1 discharges fast through D_1, terminating the ramp.

Without Q_1, ramp slope is determined only by C_1, R_2 and the voltage level of FF_1's Q output. Any change in this voltage, caused by power supply variations and/or transients, will produce ramp inaccuracies. Using Q_1 and R_2 as a constant-current source isolates the output ramp voltage from supply irregularities.

Linear ramp generator. Constant-current source, formed by FET Q_1 and resistor R_2, enables precision ramp generator to supply very linear output. Input trigger sets FF_1, whose output is integrated by amplifier Q_1, C_1, and R_2 to produce a ramp. Constant current makes ramp insensitive to supply variations. Comparator logic, external to generator, terminates ramp with pulse that resets flip-flop FF_1.



Logic signals pulse heaters for multiplexed display

by Eric Breeze
Fairchild Semiconductor, Mountain View, Calif.

Seven-segment fluorescent readout tubes can be multiplexed with a heater supply that operates from 5-volt logic levels. Because of thermal inertia, pulsed power keeps the filament hot during the pulse off-period.

Basically, the readout is a vacuum tube diode with seven phosphor-coated anodes. When a positive potential is applied between the cathode and an anode, electrons strike that anode, activating the phosphor. To use the readout in a multiplexing mode, both its anodes and cathode must be addressed.

Since the tube's heater acts as the cathode, it is difficult to supply power to one heater and isolate it from the others. The solution is to use logic signals with a one-eighth duty cycle (for an eight-digit display).

The circuit shown is for eight multiplexed digits, but it can easily be changed to six digits by modifying the scan counter. Each of the heaters has a transistor, a diode, and a resistor associated with its supply. When the transistor conducts, the readout is active. When the transistor is off, the resistor pulls the cathodes up to the positive supply potential, reverse-biasing the diode and leaving no potential across the tube.

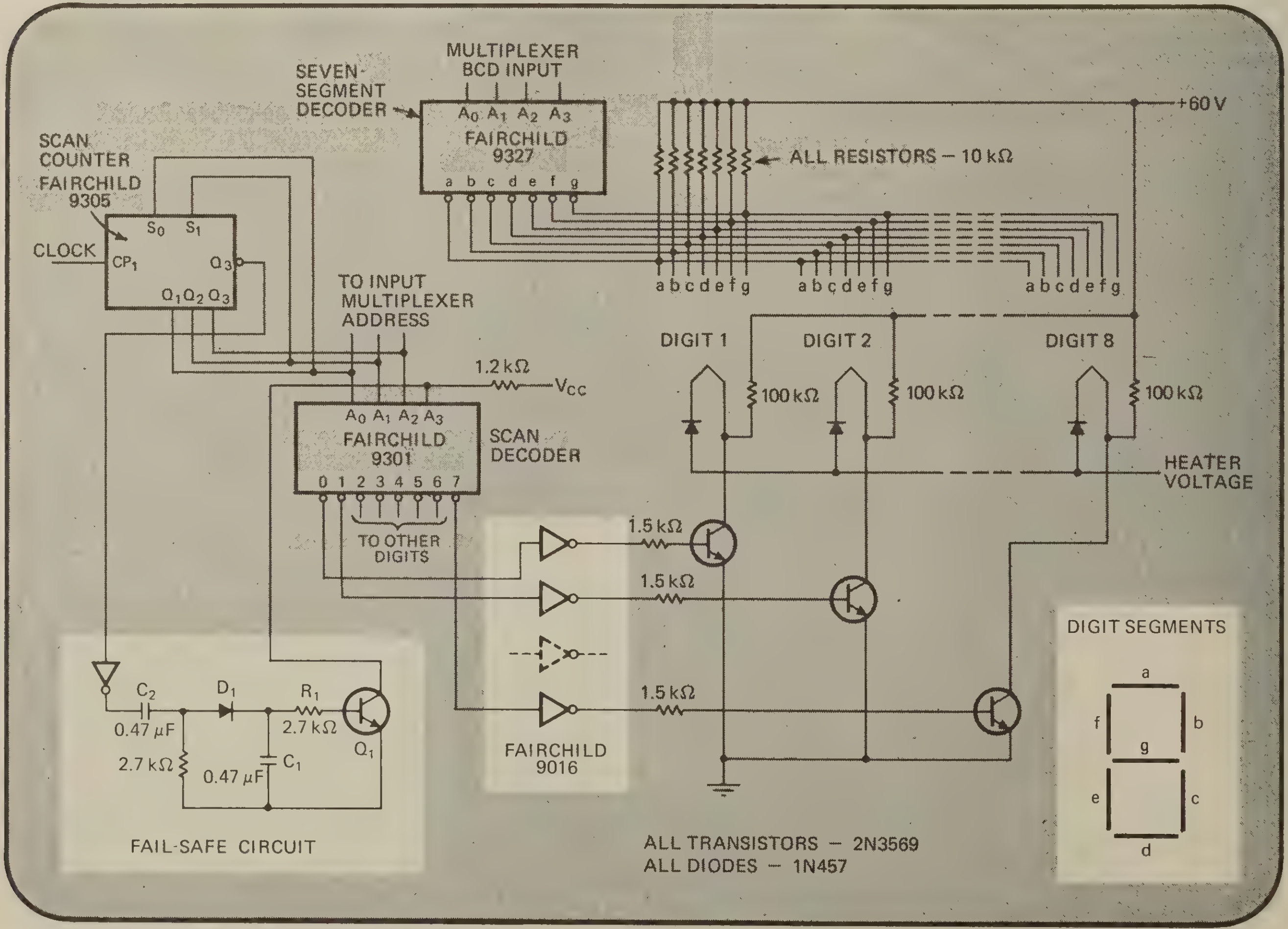
To find the total filament voltage (V_R) required for pulse-mode operation, use:

$V_P = N_{\leftarrow}V_F$ + diode and switching losses, where N is the number of parts in the scan cycle, and V_F the tube filament voltage. If Sylvania, Tung-Sol, or General Electric readouts are used, $V_F = 1.4$ v. For the eight-digit ($N = 8$) display shown:

$V_P = 8_{\leftarrow}(1.4) + 0.9 = 4.9$ V

In the event of clock failure, a fail-safe circuit on the most-significant bit of the scan decoder prevents the full filament supply voltage from being applied to any one heater. As long as the counter is operating, pulses to diode D_1, resistor R_1, and capacitor C_1 bias transistor Q_1 on. Clock failure removes the bias from Q_1, changing the input code to the scan decoder so that the decoder's unused outputs are addressed. Ac coupling through capacitor C_2 is necessary in case the counter output should stop in the high condition.

Eight-digit display. Filament supply for multiplexed seven-segment readout tubes is controlled by logic signals. Pulses of heater power keep tubes operating even during pulse off-period, and the filaments remain isolated from each other. Fail-safe circuit prevents individual filaments from receiving full heater supply voltage if the clock fails. Clock frequency can be as high as 20 kilohertz.



Positive and negative gates trim logic package count

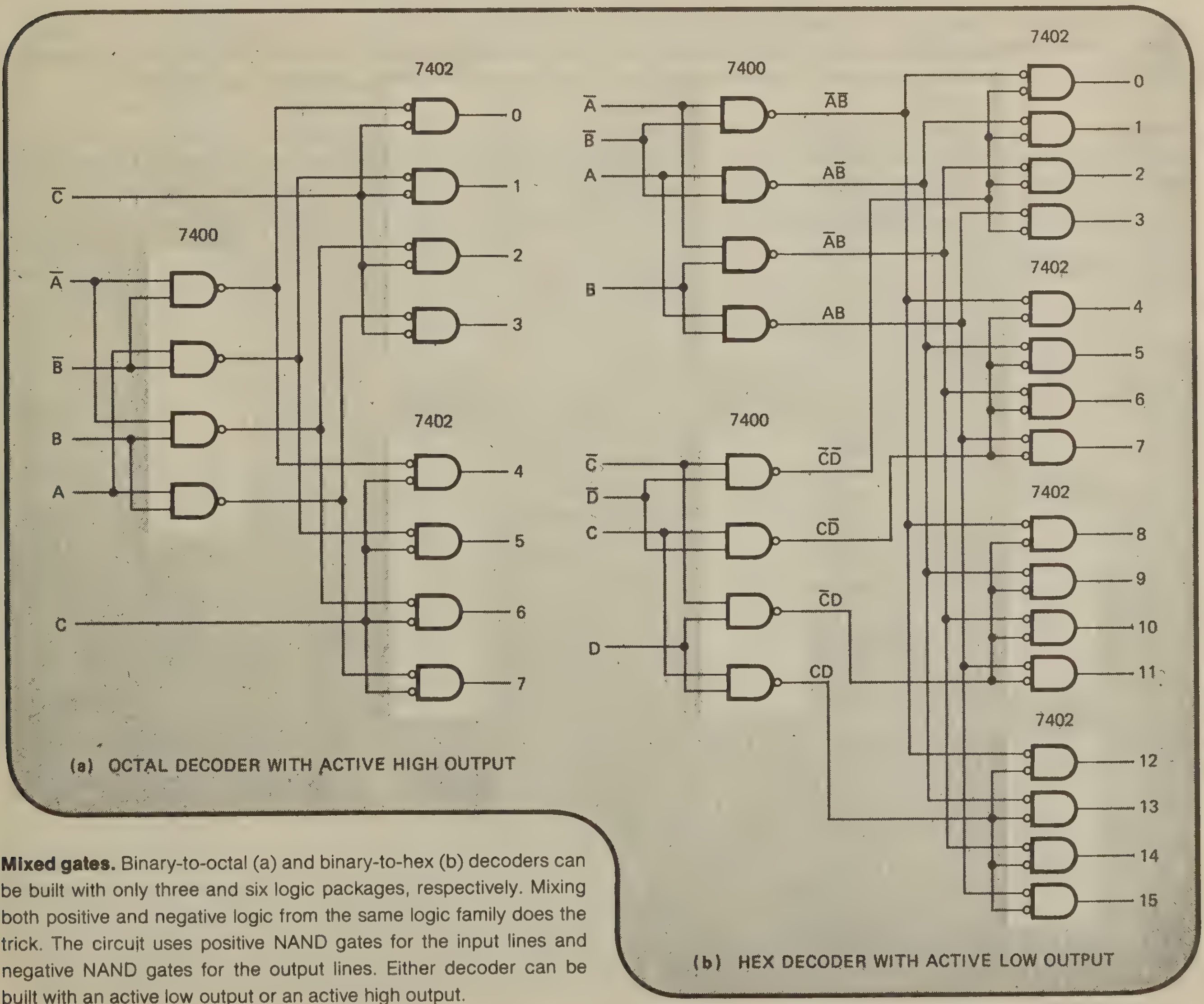
by Louis E. Frenzel Jr.
National Radio Institute, Washington, D.C.

The number of logic packages needed to implement a decoding function can be significantly reduced, and costs can be held down, by mixing and matching individual gates to build your own decoder. The scheme is effected by mixing positive and negative gates from the same logic family. Package count is reduced because the mixed logic uses a tree or cascade decoding arrangement.

Normally, five type-7410 positive NAND gates (each 7410 package contains three triple-input NAND gates) are required to realize a binary-to-octal decoder with an active low output. A decoder with an active low output produces a binary 0 at the selected output, while all other outputs are at binary 1. Additional inverter packages are required to achieve an active high output.

The circuit of (a) uses only three IC packages to realize the same decoding function, but with an active high output. Four dual-input positive NAND gates decode least-significant bits A and B; two quad dual-input negative NANDs provide the final decoding for the C bit.

This positive-negative mixing technique can also be applied to a hex decoder. Ordinarily, eight type-7420 positive NAND gates (each 7420 package consists of two four-input NAND gates) are needed for a one-of-16 hex decoder that has an active low output. However if positive NAND gates are mixed with negative NANDs, only six ICs are needed (b).



Mixed gates. Binary-to-octal (a) and binary-to-hex (b) decoders can be built with only three and six logic packages, respectively. Mixing both positive and negative logic from the same logic family does the trick. The circuit uses positive NAND gates for the input lines and negative NAND gates for the output lines. Either decoder can be built with an active low output or an active high output.

High-impedance driver boosts detector's dynamic range

by Robert J. Matheson
U.S. Department of Commerce, Office of Telecommunications, Boulder, Colo.

Most detectors have a limited dynamic range of around 40 decibels because the diodes they employ do not conduct effectively when diode voltage falls below 0.1 to 0.5 volt. By driving the diodes with a high-impedance current source, the dynamic range for a full-wave detector can be increased to 120 dB.

Although diodes do not detect efficiently below their threshold voltage, they can conduct a very small current. The high-impedance driver, then, performs like an ideal current source, always forcing the proper current through the diodes regardless of diode voltage. Hot-carrier diodes are used in the detector shown since their threshold voltage is lower than that of ordinary diodes (0.1 to 0.2 V, rather than 0.5 V).

Commonly, detector dynamic range is increased by driving the diodes from a high-voltage step-up transformer. However, this technique is limited by diode reverse breakdown voltage and produces only about a 60-dB range. Operational amplifiers are often added to the circuit to broaden detector dynamic range, but they restrict operation to relatively low frequencies.

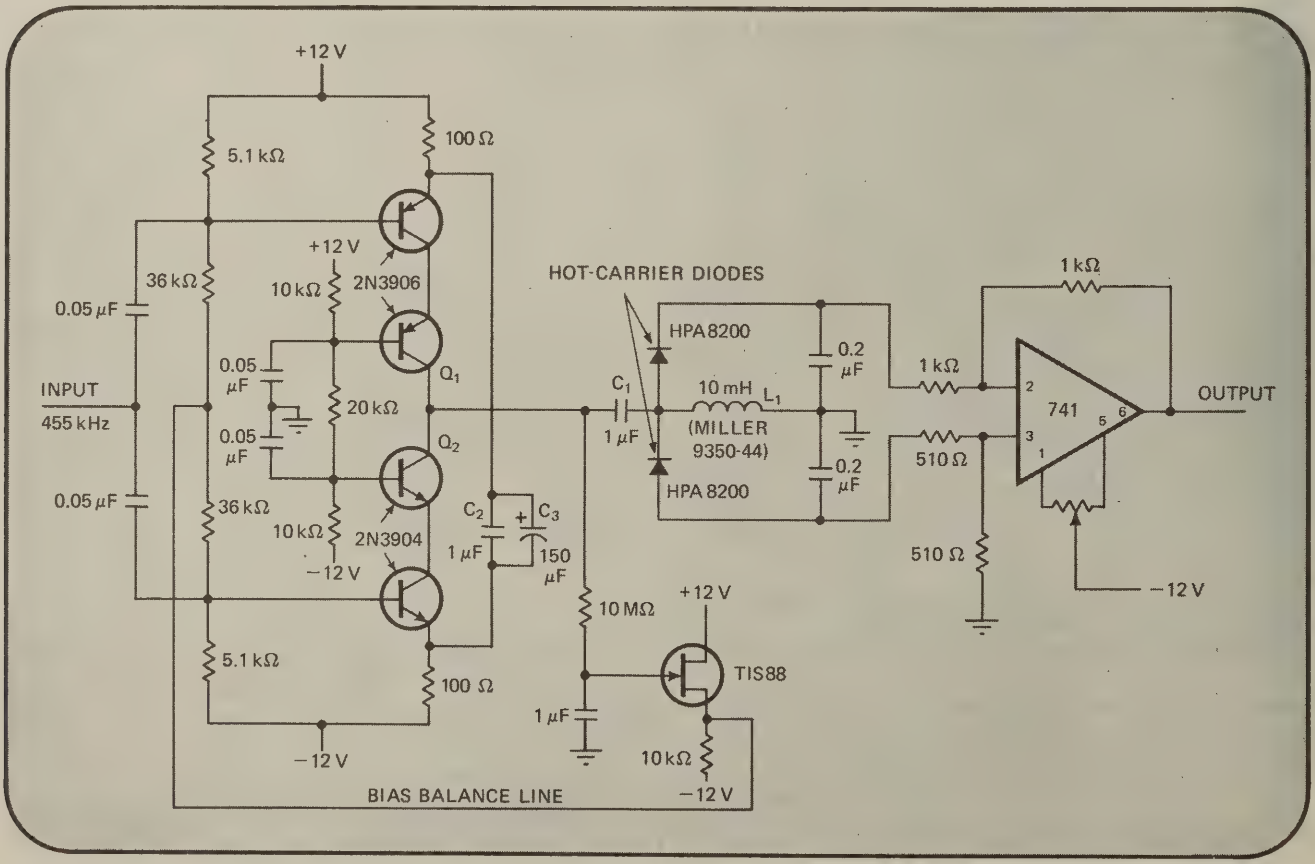
In the wide-range detector, two transistors, biased in a complementary common-base configuration, are the basic driving components. Transistors Q_1 and Q_2 provide an output impedance of about 2 megohms at a capacitance of 10 picofarads. Inductor L_1, which has an equivalent parallel resistance between 500 kilohms and 1 megohm, tunes out this capacitance. (The inductor should be kept out of a direct current path since any dc flow may significantly reduce its parallel resistance.)

Because the driver stage operates at an extremely high impedance level, even a minute direct current imbalance (due to component tolerances) introduces a large voltage change that could force either Q_1 or Q_2 into saturation. An FET source-follower prevents this by balancing the bias currents in each half of the driver. The hot-carrier diodes are isolated from any net dc imbalance at the driving point by capacitor C_1.

Both positive and negative half-cycles of the input signal are detected by the diodes, resulting in full-wave detection. The detected signal has a ripple frequency of 910 kilohertz, which is smoothed by a low-pass filter and a differential amplifier buffer. Capacitors C_2 and C_3 improve detector large-signal performance, particularly for short-duration pulses.

For a 455-kHz input, detector output is linear from 10 millivolts to 10 V. From 10 microvolts to 10 mV, the output deviates slightly from linearity, with a maximum deviation of 0.1 dB for an input change of 1 dB.

Full-wave detector. Complementary four-transistor array forms high-impedance driver that forces desired current through hot-carrier diodes. FET source-follower balances driver bias current to prevent unwanted transistor saturation. Diodes detect positive and negative portions of input signal, which is then filtered and buffered. Detector operates over 120-decibel dynamic range for 455-kilohertz input.



Analog-digital circuit turns scope into curve tracer

by Robert D. Guyton
Mississippi State University, State College, Miss.

Any standard oscilloscope having a vertical differential amplifier input can easily be made to function as a transistor curve tracer. With an inexpensive analog-digital circuit, the common-emitter characteristics of npn transistors can be displayed, and with two slight modifications pnp transistors also can be accommodated.

The circuit generates two waveforms: a staircase step function (V_B) to drive the transistor's base, and a triangular wave (V_C) for the collector. A pair of RTL $\bar{J}$-$\bar{K}$ flip-flops and two operational amplifiers are the major circuit components.

Flip-flops FF_1 and FF_2 form a binary counter output is summed by op amp A_1. The output of A_1, a four-step staircase voltage, supplies the base drive. Additional voltage steps can be added by increasing the number of flip-flops and summing resistors.

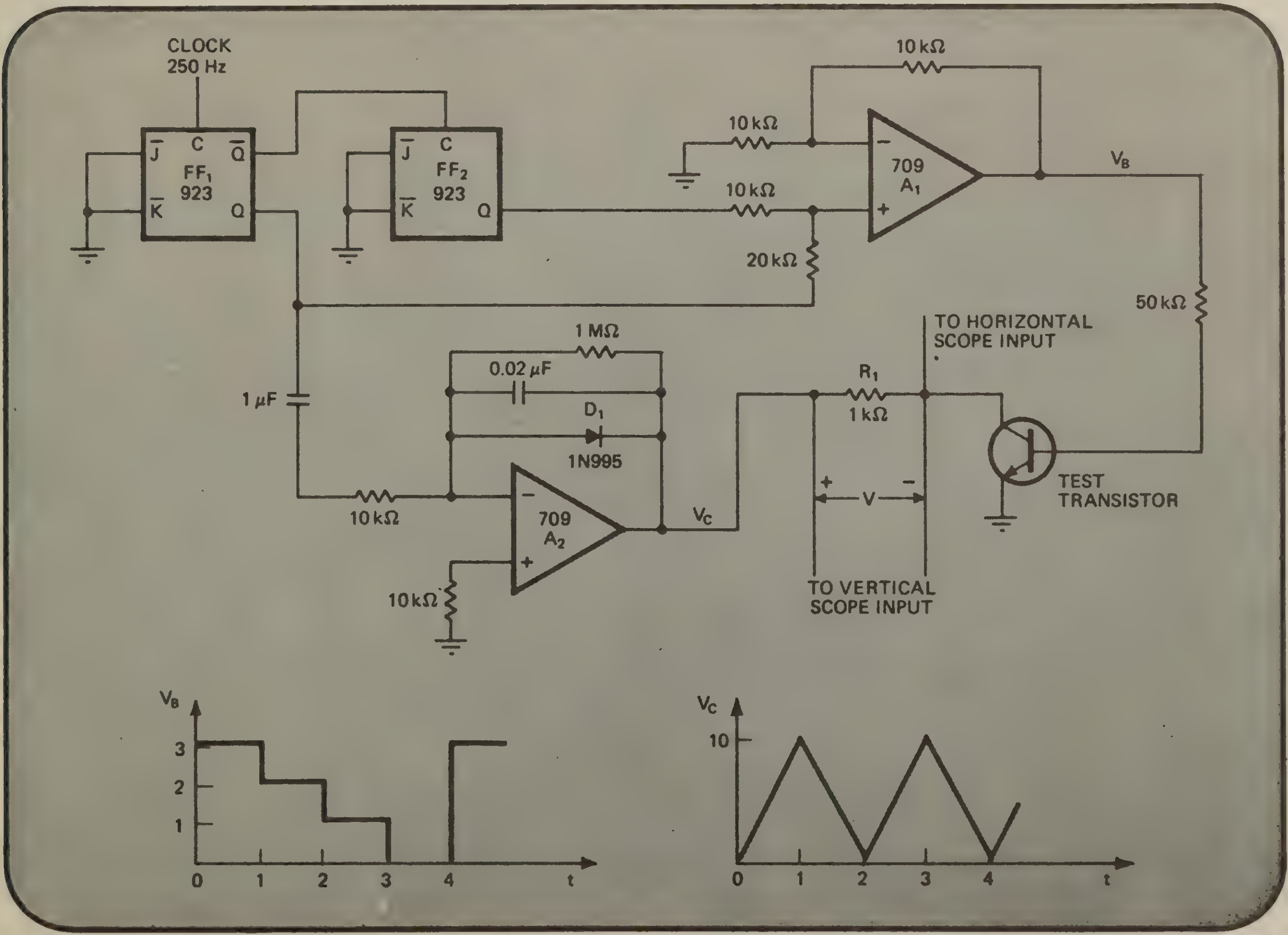
The output square wave of FF_1, when integrated by op amp A_2, provides the triangular collector voltage. The amplitude of this voltage is controlled by an input clock frequency; the higher the frequency, the smaller the amplitude. Diode D_1 clamps the waveform to a positive swing so that the test transistor is protected against a wrong voltage polarity.

Collector current is determined by measuring the voltage across the collector supply resistor, R_1. For example, if R_1 = 1 kilohm and the scope's vertical attenuator is set to 1 volt per centimeter, the vertical current scale is calibrated at 1 milliampere per centimeter, and the horizontal voltage scale to 1 volt per centimeter.

Circuit current and voltage ranges are limited by amplifiers A_1 and A_2. Tacking a power transistor on the output of each op amp is a simple way to extend the circuit's operating range.

To display the characteristics of a pnp transistor, the output of FF_2 must be summed at the negative input of A_1 to invert the staircase voltage, and diode D_1 must be reversed to clamp the triangular wave to negative voltages. Or, adding a multiposition switch to accomplish these changes would permit checking either transistor type with just the flick of a switch.

Curve tracer. Inexpensive circuit allows common-emitter characteristics of npn transistor to be displayed with ordinary scope. Output of binary counter (FF_1 and FF_2) is summed by A_1 to generate staircase base drive (V_B) for test transistor. Triangular collector drive (V_C) results when square-wave output from FF_1 is integrated by A_2. Transistor voltage-current curve is displayed by using voltage across R_1.



One-of-eight decoders test and correct parity

by Michael J. Gordon, Jr.
Psynexus Systems, Wilmetter, Ill.

Only four one-of-eight decoder packages are all it takes to build an eight-bit parity checker that also can be used for parity correction. Either odd or even parity testing can be done.

The basic circuit can be adapted to suit almost any logic family; complete data is given for TTL and MOS packages. When wired as indicated, the decoders produce a logic 0 output for correct parity, a logic 1 output for incorrect parity.

Suppose the input word is 10111001, and it is to be checked for even parity. Since there is an odd number of 1s, a parity error should be indicated. The three least-significant bits become the I_0, I_1 and I_2 inputs. The next three bits, going from right to left, are inputs I_3, I_4 and I_5. The last two bits become I_6 and I_7.

Because decoder D_1 receives only a single 1, its output is 1. The input to D_2 contains three 1s, causing another parity error. Decoder D_3 also produces a 1, since its input contains just one 1. Three 1s, therefore, are applied to D_4, resulting in a 1 output, indicating a parity error.

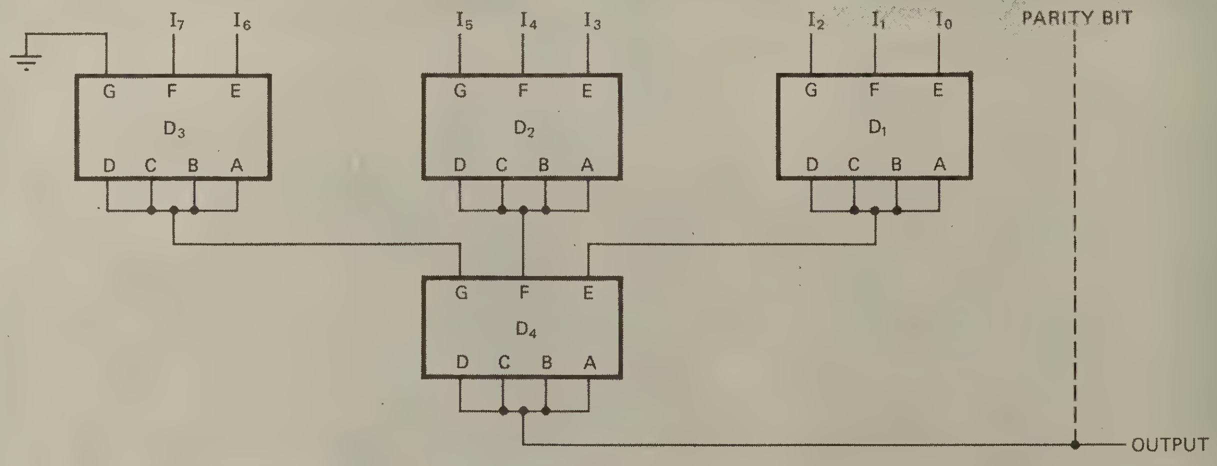
If the input word has correct, even parity, the output will be a 0. Let the word be 10010110. Now D_1 produces a 0, D_2 a 1, and D_3 a 1. Since the input to D_4 contains an even number of 1s, the output is 0, indicating correct parity.

Using the output as the parity bit corrects any parity error. If the circuit is wired for even parity, there will always be an even number of 1s. When wired for odd parity, the circuit will always supply an odd number of 1s.

For example, if the seven-bit word 1101101 is checked for even parity, the circuit's 1 output can become the eighth bit to correct the parity error. Of course, whenever word parity is correct, the circuit produces a 0, which does not change parity.

The outputs of the decoders shown in the diagram are wire-ORed together. If the decoder package used does not have this feature, an OR gate must be added to its output.

Testing, testing. Eight-bit parity checker generates a logic 0 for correct parity, a logic 1 for incorrect parity. Decoders D_1, D_2 and D_3 accept input data word and supply three-bit input for output decoder D_4. Circuit can test for either odd or even parity, depending on how it is wired. An OR gate must be added to output of each decoder if the type of logic employed cannot be wire-ORed.



DECODER	LOGIC	PARITY	PACKAGE PIN NUMBERS						
			A	B	C	D	E	F	G
MOTOROLA MC4038P	TTL	ODD	13	2	4	11	15	6	1
		EVEN	3	5	12	14	15	6	1
MOTOROLA MC1150L	MOS	ODD	2	5	12	13	15	9	7
		EVEN	4	3	11	14	15	9	7

With feedback, isolation amp gives better-than-unity gain

by Roland J. Turner
RCA Corp., Missile and Surface Radar division, Moorestown, N.J.

An isolation amplifier with degenerative feedback provides gain over a large bandwidth, yet keeps output impedance low. An amplifier set up this way can be an excellent driver for long, low-impedance transmission lines or other highly capacitive loads. The circuit can even be used as a gate when its dual MOSFET is driven to cutoff. (Conventional isolation amplifiers, like emitter-followers, are usually unity-gain circuits.)

Moreover, gain and output impedance in the improved amplifier are insensitive to variations in the MOSFET's transconductance (g_m) and the bipolar transistor's beta (β). Normally, g_m drops by a factor of three as temperature rises from room conditions to 60°C, while β increases with rising temperature. In this amplifier, the changes in g_m and β can offset each other.

Gain is 17 decibels from several kilohertz to 20 megahertz; output impedance is less than 10 ohms. Furthermore, isolation greater than 50 dB can be achieved at frequencies as high as 6 MHz. The circuit's input can be operated either matched or unmatched.

As can be seen from the diagram, MOSFET Q_1 has two control gates. When the bias (V_{G2S}) of the second control gate (G_2) is decreased from 4 to –3 V dc, the forward gain through gate G_1 can drop by 50 dB, without adversely affecting its input characteristics. As V_{G2S} becomes negative, Q_1 is driven into pinchoff, reducing its drain current. Transconductance through the signal gate then drops from 15 millimhos to 50 micromhos.

The voltage transfer function for the amplifier is:

$$\frac{e_o}{e_i} = \frac{g_m[\beta R_1 + (\beta + 1)R_2]}{1 + g_m(\beta + 1)R_2}$$

which indicates that amplifier gain is directly proportional to g_m. If $g_m(\beta + 1)R_2$ is greater than 1, e_o/e_i reduces to:

$$\frac{e_o}{e_i} \simeq \frac{1}{1 + 1/g_m(\beta + 1)R_2} + \frac{R_1}{R_2}$$

and circuit output impedance becomes:

$$Z_o = \frac{1}{g_m(\beta + 1) + 1/R_2} + \frac{R_1}{\beta + 1}$$

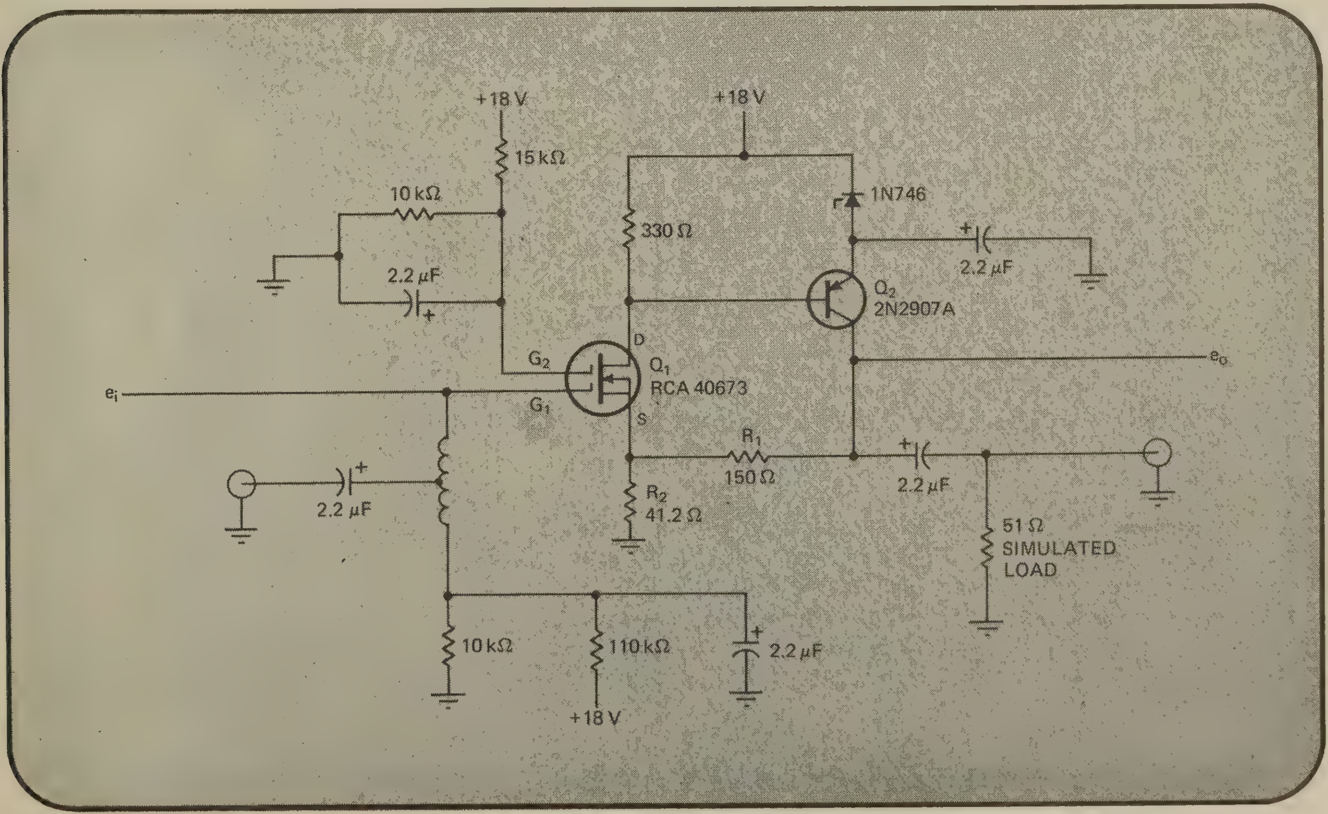
which equals $R_1/^b$ for frequencies to 10 MHz.

As Q_1 approaches pinchoff, its drain current drops, thereby driving Q_2 towards cutoff. Since Z_o increases as β decreases, amplifier gain is effectively reduced by mismatch. In the limit, as both g_m and β approach 0:

e_o/e_i approaches $1 + R_1/R_2$, and
Z_o approaches $R_1 + R_2$.

The input transmission-line transformer is similar to a Z-match type 50-200E. If the secondary of the transformer is terminated with 200 ohms, a low input VSWR can also be realized. Total parts cost is less than $5.

Line driver. Isolation amplifier makes ideal line driver. It supplies more than unity gain while holding output impedance under 10 ohms through frequencies as high as 20 megahertz. Degenerative feedback through Q_2 makes circuit performance insensitive to device parameter changes. Bias of Q_1's control gate G_2 effects gating action without harming input characteristics of signal control gate G_1.



Diode and SCR protect multiple-voltage equipment

by Peter T. Uhler
Midwest City, Okla.

Placing a diode between two different power supply lines permits one low-power SCR to control both supplies, thus protecting components from an overvoltage condition. Often, several supply voltages must be used to power a single piece of equipment, creating a hazard for those circuits that operate from a low voltage. If critical components fail, or if two or more supplies are accidentally shorted, these low-voltage circuits are usually destroyed.

Multiple-voltage protection is quite important for equipment containing integrated circuits, since ICs generally operate from low-voltage supply lines. The circuit shown is intended primarily for overvoltage protection—overcurrent protection is secondary in this case.

The voltage at point A or B determines when the SCR fires. Transistors Q_1 and Q_2 act as current-sensing elements. Resistor R_1 and diode D_1 trigger Q_1 at around 250 milliamperes, as do R_2 and D_2 for transistor Q_2. The SCR requires only about 5 microamperes to trigger it.

In the event of a fault (when the output currents of Q_1 and Q_2 exceed 250 mA), the SCR fires, turning transistor Q_3 off. Diode D_3 then turns off transistor Q_4, thereby permitting two supplies to be controlled by one SCR. More than two supplies can be controlled by a simple extension of this basic technique.

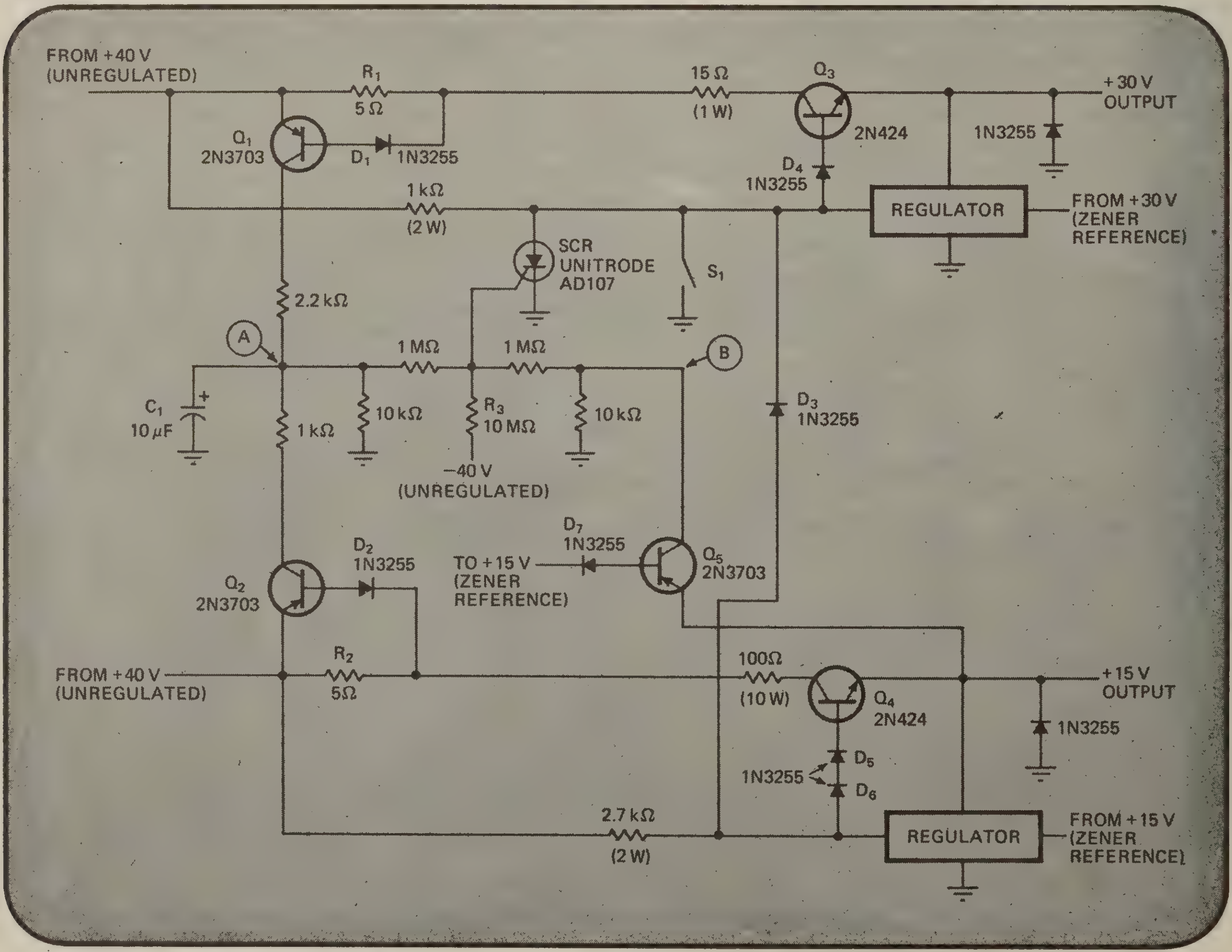
Diodes D_4, D_5, and D_6 assure that transistors Q_3 and Q_4 are turned off completely. Capacitor C_1 at point A provides a time delay of about 0.1 second so that initial load-current surges will not trigger the SCR.

Should the 15-volt supply rise about 16.4 V, transistor Q_5 fires the SCR immediately since there is no capacitor at point B. Diode D_7 protects Q_5 if the 15-V supply becomes shorted.

Premature triggering of the SCR due to its differential voltage (dv/dt) effect is prevented by resistor R_3. Switch S_1, which should be part of the power control switch, resets the SCR after the supplies are turned off.

Approximate parts cost for the protection portion of the circuit shown is $10.

Double protection. Overvoltage protection circuit monitors 15- and 30-volt supply lines at the same time. Because supplies are interconnected with diode D_3, only one SCR is needed. If output currents of Q_1 and Q_2 exceed 250 milliamperes, SCR fires, turning Q_3 off, while D_3 turns Q_4 off. Q_5 can also trigger SCR if 15-V supply reaches 16.4 V. Capacitor C_1 prevents transient current overloads from firing SCR.



Dual op amp comparator controls ramp reference

by Ronnie Jack McKinley
Duncan, Oklahoma

A control comparator can be used to establish the end points of a sawtooth generator's ramp output. That way, the sawtooth's end points don't drift with temperature, providing a stable output. The ramp, which travels from absolute zero potential to 5 volts, can be varied over a frequency range of 0.33 hertz to 1 kilohertz.

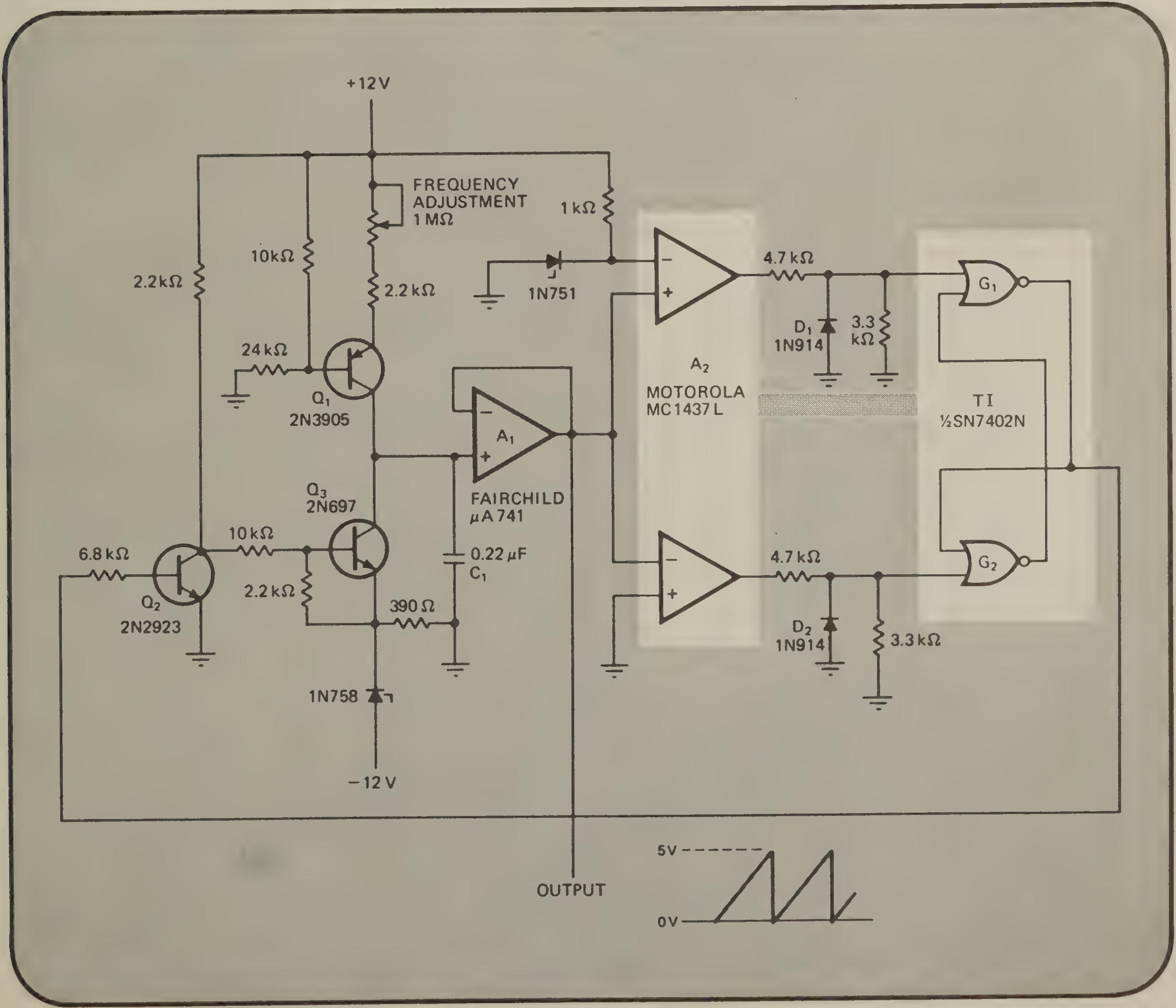
Constant-current source Q_1 linearly charges capacitor C_1, whose voltage is buffered by unity-gain follower A_1. Comparator A_2 is formed by two operational amplifiers operating at open-loop gain; a flip-flop is realized from NOR gates G_1 and G_2. Diodes D_1 and D_2 prevent gate inputs from becoming more negative than –0.5 V, while the 4.7- and 3.3-kilohm voltage dividers stop the gate inputs from exceeding 5 V.

The comparator sets up two threshold reference points—one at absolute zero potential, the other at 5 V. When the voltage across C_1 reaches 5 V, A_2 switches, causing the flip-flop to produce a negative pulse. This turns Q_2 off and Q_3 on so that C_1 discharges.

Since Q_3's emitter is biased at –2 V, the discharging capacitor tries to reach V_{SAT} –2 V. However, when the voltage across C_1 becomes zero, the comparator switches, returning the flip-flop to its original state.

Transistor Q_2 now conducts, Q_3 goes off, C_1 begins charging again from a stable zero point, and the cycle repeats. Because of the comparator reference, the baseline of the ramp cannot be shifted by any temperature variance in the V_{SAT} of Q_3.

Supplying temperature-stable output. Dual comparator in this sawtooth generator sets lower and upper end points of ramp. Constant current from Q_1 charges C_1 until the capacitor's voltage becomes 5 V. Comparator A_2 then switches, toggling flip-flop formed by G_1 and G_2. Q_2 turns off, Q_3 turns on, and C_1 discharges until its voltage is zero. Then A_2 switches again, triggering the flip-flop, which turns Q_2 on and Q_3 off.



One-shot makes fast trigger out of slow input pulse

by Raymond J. Manco
Foxboro Co., East Bridgewater, Mass.

In addition to being insensitive to transients, a hybrid monostable multivibrator can trigger high-speed integrated circuit flip-flops with either a slowly rising or slowly falling pulse of an input. The triggering device may be a logic circuit, a relay, a toggle switch, or a momentary-contact pushbutton switch. The one-shot can even be made variable by adding a biasing resistor.

Most IC flip-flops require transient-free trigger pulses with fast rise times. The circuits shown in (a) and (b) generate a pulse whose rise time is 10 to 100 nanoseconds and whose duration is 10 microseconds. Rise time for the trigger input can be 10 ns to 10 milliseconds.

The one-shot configuration of (a) should be used when the input is a slowly rising pulse. It is triggered by the leading edge of the input pulse, which turns on transistor Q_1. Gate G_1 is then enabled, and transistor Q_2 switches on. Feedback from Q_2's collector to G_1's input keeps the gate high whenever Q_2 is on so transients in the input trigger do not influence the one-shot.

Gate G_2, which is enabled by Q_2, shapes the monostable's output pulse for triggering a high-speed TTL micrologic bistable, like the 9001 J-K flip-flop shown.

If the flip-flop being triggered requires a negative-going pulse, the output of G_2 can be inverted with a third type 9002 NAND gate. Trailing-edge triggering also can be implemented with series 54/74 TTL ICs, as illustrated in (b), or with DTL gates.

The circuit action of (b) is similar to that of (a), although a relay contact provides the input trigger pulse. The input pulse's trailing edge enables the first NAND gate, which turns on the transistor. A feedback loop again keeps the gate on while the transistor conducts. Two more NAND gates, one shaping and the other for inverting the pulse, result in a negative spike input for the SN54L72 J-K master-slave flip-flop.

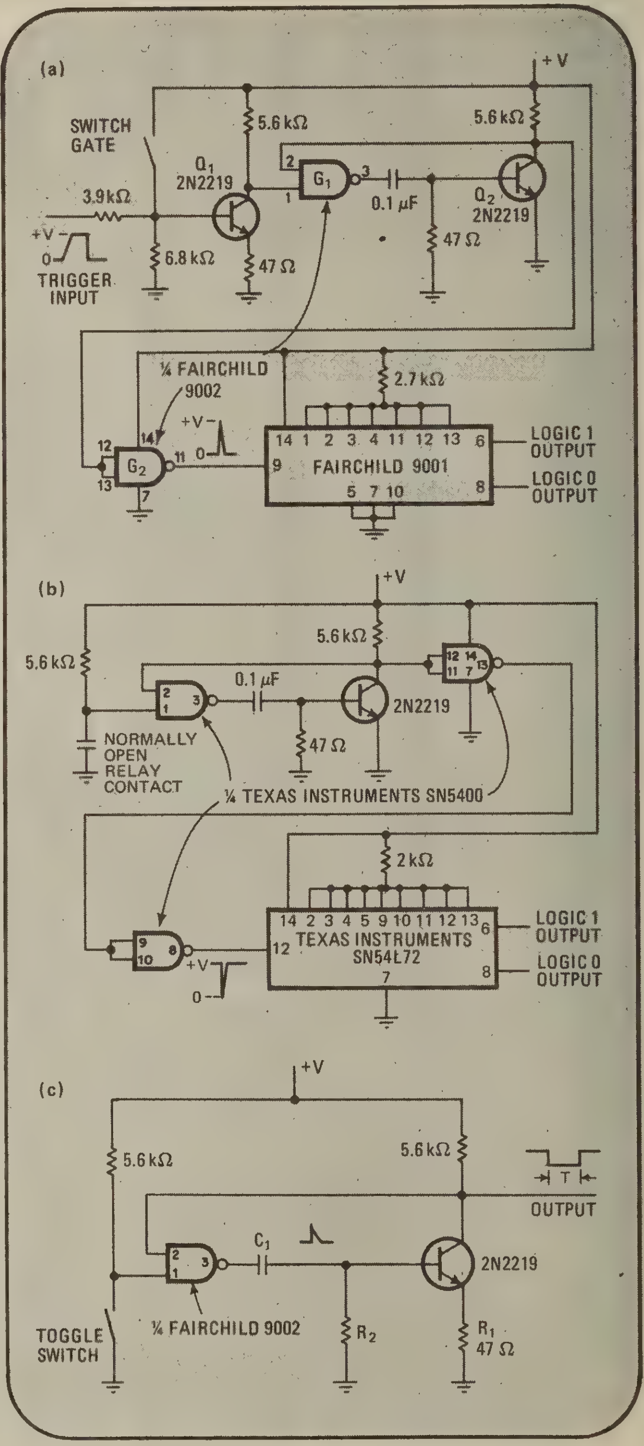
The circuit of (c) shows how output pulse width can be expanded from 10μs to 25 ms. This variable oneshot requires a toggle switch input, one NAND gate, and one transistor with feedback to the gate. Adding R_1 (47 ohms) between the transistor's emitter and ground causes the transistor's input resistance, R_i, to be greater than R_2, or:

$R_i = \beta R_1$ where β is transistor current gain. Output pulse width becomes:

$T = 5 C_1 R_2 R_i/(R_2 + R_i)$

Resistor R_2 can range from 10 ohms to 100 kilohms, and capacitor C_1 from 0.1 microfarad to 1 ${}_x$F.

Pulse shaper. Hybrid one-shot uses NAND gates and a transistor to deliver sharp positive-going or negative-going spike from slowly rising pulse (a) or slowly falling pulse (b). Input transients do not affect output triggering because of feedback from transistor to preceding gate. Adding a resistor to transistor's emitter loop, as shown in (c), permits output pulse width to be varied.



FET supply tests bipolar current gain

by James B. Marshino
CTS Microelectronics Inc., Lafayette, Ind.

With just a simple, variable constant-current source, it's easy to measure direct current gain for a bipolar transistor with better than 1% accuracy. The source controls both collector and base currents with only four active devices—a differential operational amplifier, two field effect transistors, and a diode. In addition, the circuit also can be used for go/no-go testing with slight modification. Approximate parts cost is about $10.

When power is first applied, Q_1 is on, Q_2 is off, and the bipolar transistor is also off because no base current can flow. As current through R_1 increases, voltage at the noninverting input of comparator A_1 rises.

The threshold voltage of A_1, which is determined by R_2 and the setting of potentiometer R_3, fixes the bipolar's collector-emitter junction potential. When the bipolar's collector voltage approaches A_1's threshold, the amplifier switches and its output goes low.

This decreases the gate-source voltage of Q_1, thus limiting the flow of current through diode D_1 and decreasing the voltage across resistor R_4. FET Q_2 now turns on and operates in its active region. Since the time constant of R_4 and C_1 is large, Q_2 sees these components as a constant voltage source.

A small constant current, then, flows in the base loop of the bipolar being tested, turning that device on. Because the base current (I_B) is constant, the transistor's collector current (I_C) is also constant, permitting accurate determination of current gain.

The magnitude of I_B can be measured directly with a voltmeter by reading the voltage across resistor R_5 (V_{R5}):

$$I_B = V_{R5}/R_5$$

Transistor collector-emitter voltage (V_{CE}) and I_C are determined from the manufacturer's data sheet:

$$-V_{CC} = V_{CE} + R_1 I_C$$

where $-V_{CC}$ is the collector supply voltage. Or I_C can be measured directly by using the voltage across resistor R_1. The dc current gain (h_{FE}) becomes just a matter of division:

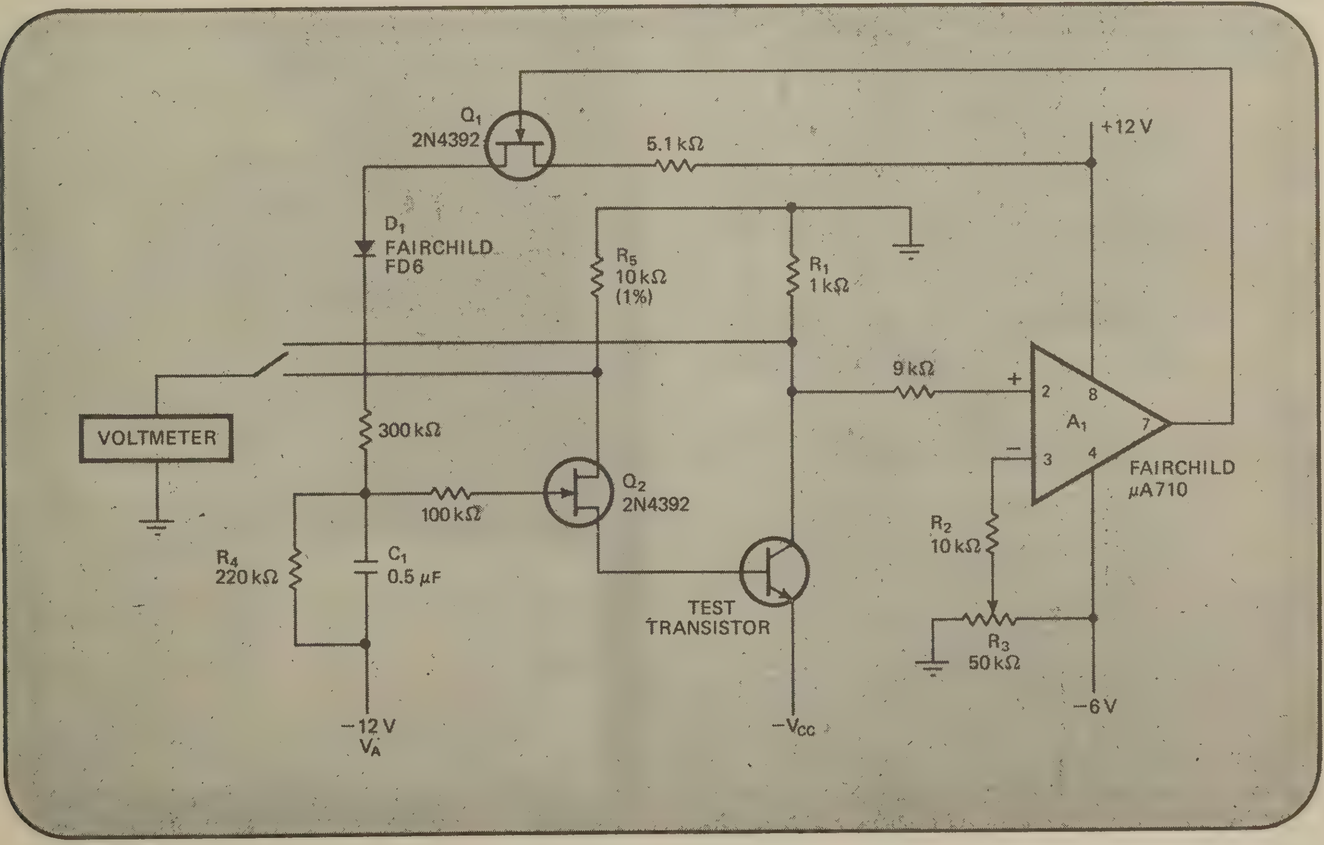
$$h_{FE} = I_C/I_B$$

To use the circuit as a go/no-go tester, replace the voltmeter with a Fairchild type μA711 dual limit detector. Increased measurement accuracy can be obtained by putting an operational amplifier between the circuit and the detector.

The test circuit illustrated is for an npn transistor. One caution should be observed: the V_A supply must be more negative than the $-V_{CC}$ supply to keep Q_2's gate-source junction reverse-biased.

To check a pnp transistor, supply polarities must be reversed and p-channel FETs used.

Measuring current gain. Amplifier A_1, and FETS Q_1 and Q_2 form constant-current supply for testing h_{FE} of bipolar transistor. When bipolar's collector voltage approaches A_1's variable threshold, A_1 goes low, decreasing current through D_1. Constant voltage provided by large R_4C_1 time constant also drops so that Q_2 conducts. Bipolar now turns on with controlled constant I_B and I_C, which are measured with a voltmeter.



Feedback pot extends multivibrator duty cycle

by Michael J. Shah
University of Wisconsin, Madison, Wis.

It's easy to design an astable multivibrator that has a variable duty cycle of 1% to 99%. Just put a pair of diodes and a linear potentiometer in a feedback loop to the inverting input of a differential operational amplifier and add a positive feedback resistor for regenerative action. The configuration requires only one timing capacitor and features good temperature stability. Moreover, variation in duty cycle is nearly independent of repetition rate. The op amp performs as a comparator, switching from one state to another when its input voltages are equal.

Let e_o be the astable's output voltage, e_1 the voltage at the comparator's inverting input, and e_2 the voltage at the non-inverting input. When e_o is the maximum output voltage (V_{SAT}) of the op amp, where V_{SAT} approximately equals $V_{CC}- 0.5$, diode D_1 is forward-biased, and diode D_2 is reverse-biased. Timing capacitor C_1 is charging towards V_{SAT} through D_1, KR_1 and R_2. (K is a constant whose minimum value is 0 and maximum value is 1.)

As can be seen from the circuit diagram of (a), e_2 is determined by voltage division across R_3 and R_4:

$$e_2 = R_4 V_{SAT}/(R_3 + R_4) = V_{SAT}/2$$

since $R_3 = R_4 = 100$ kilohms. When e_1 reaches $V_{SAT}/2$ at time t_1 (due to the charge across C_1), the comparator switches, bringing e_o from V_{SAT} to $-V_{SAT}$. Diode D_2 becomes forward-biased, and diode D_1 reverse-biased.

The capacitor now charges towards $-V_{SAT}$ through D_2, $(1 - K) R_1$, and R_2. Voltage e_2 is again determined by voltage division across R_3 and R_4:

$$e_2 = R_4(-V_{SAT})/(R_3 + R_4) = -V_{SAT}/2$$

When C_1 discharges sufficiently to make e_1 equal to $-V_{SAT}/2$ at time $t_1 + t_2$, the comparator switches back to V_{SAT}, C_1 begins to charge, and the cycle repeats. Resistor R_3 provides a positive feedback function for regeneration of the astable's cycle.

The equation for the on time, T_1, is:

$$T_1 = (KR_1 + R_2)\, C_1 \ln \left[\frac{V_{SAT} - V_{D1} + V_{SAT}/2}{V_{SAT} - V_{D1} - V_{SAT}/2} \right]$$

where V_{D1} is the voltage drop across diode D_1. The expression for the off time, T_2, becomes:

$$T_2 = [(1 - K)\, R_1 + R_2]\, C_1 \ln \left[\frac{V_{SAT} - V_{D2} + V_{SAT}/2}{V_{SAT} - V_{D2} - V_{SAT}/2} \right]$$

where V_{D2} is the voltage drop across diode D_2.

Duty cycle, D, for the astable is:

$$D = T_1/(T_1 + T_2) = (KR_1 + R_2)/(R_1 + 2R_2)$$

Minimum duty cycle occurs when $K = 0$:

$$D_{min} = R_2/(R_1 + 2R_2)$$

which approximately equals 1% for $R_{11} = 250$ kilohms and $R_2 = 2$ kilohms. Maximum duty cycle is obtained when $K = 1$:

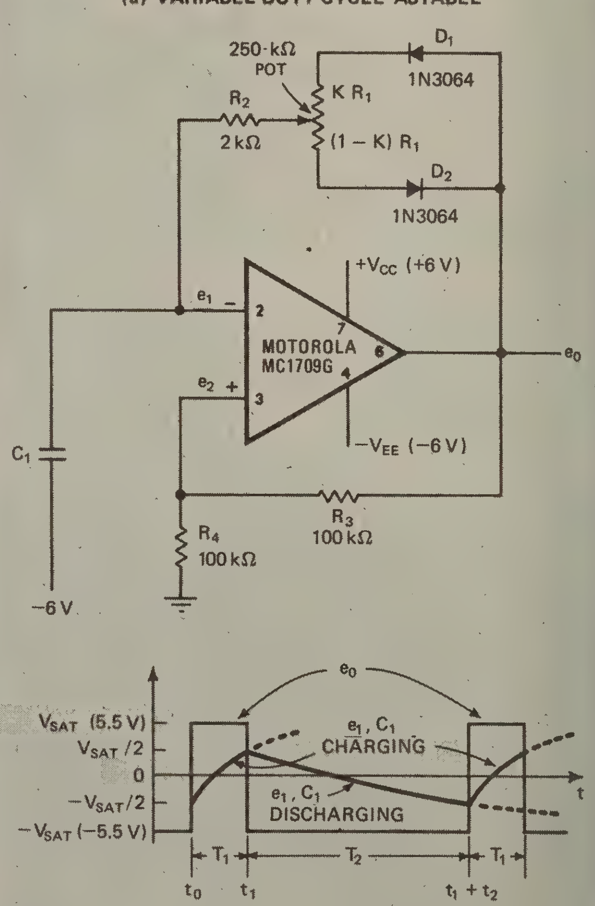
$$D_{max} = (R_1 + R_2)/(R_1 + 2R_2)$$

which approximately equals 99% for the given resistor values.

Table (b) shows circuit performance for various values of capacitor C_1.

Variable astable. Pot in comparator's feedback loop permits adjustment of astable's duty cycle over almost 100% range. When comparator output is high, D_1 conducts, D_2 is off, and C_1 charges until e_1 equals e_2. Then comparator output goes low, D_1 opens; D_2 shorts so that C_1 discharges. When e_1 is the same as e_2, the comparator switches again, and the cycle repeats. Sample data is shown in (b).

(a) VARIABLE-DUTY-CYCLE ASTABLE



(b) PERFORMANCE DATA

C_1 (μF)	$(T_1)_{min}$ (μs)	$T_1 + T_2$ (ms)	FREQUENCY (Hz)
0.0027	7	0.6	1,670
0.01	21.3	2.1	464
0.056	128	13	76.6
0.1	212	21.7	46.1
0.33	690	70.9	14.1
1	2,130	218	4.6

Variable pulse generator consists of four inverters

by Michael L. Harvey
Air Force Cambridge Research Labs, Bedford, Mass.

All that's needed to realize an inexpensive adjustable pulse generator is two-thirds of a hex inverter IC package and a few external components. Besides output frequency, the on and off times of the circuit can be varied. Frequencies as high as 500 kilohertz can be obtained with diode-transistor logic, or up to 10 megahertz with transistor-transistor logic.

When power is applied, capacitor C_1 charges and the output is low. The potential at point A increases until point B goes low, point C high, and point D low. The output now becomes high and C_1 discharges.

The voltage at point A drops until point B becomes high, point C low, and point D high. The cycle is then complete as C_1 charges while the output is low. All charge and discharge paths are inside the Fairchild type 936 DTL hex inverter. (A Fairchild 9016 TTL inverter may be used instead.)

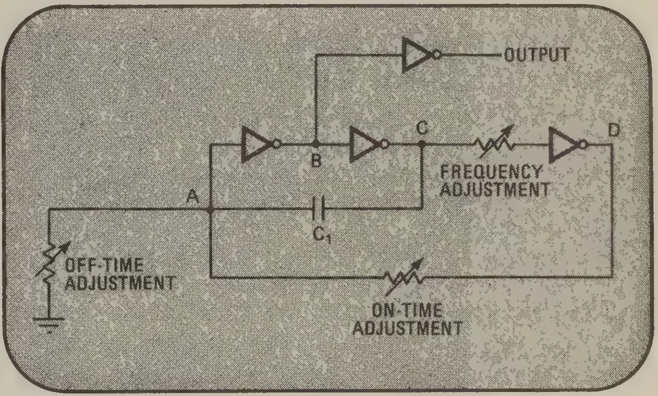
The resistor from point A to ground controls the generator's off (charge) time. Increasing the resistance decreases off time, while on time remains relatively constant. Resistance can range from 1.2 kilohms to infinity.

Similarly, the resistor between point A and point D performs as an on (discharge) control. Increasing the resistance increases on time; off time stays more or less constant. Maximum recommended resistance is approximately 2 kilohms; the minimum is a short.

Another resistor can be included, as shown in the diagram, for frequency adjustment. However, its effectiveness is limited to around a 2:1 range variation. The resistance can vary from a short to about 2 kilohms.

Capacitor C_1 can range from 0.001 to 500 microfarads. All component values are limited by minimum driving requirements for the integrated circuit.

Inverter generator. Output of pulse generator is low when C_1 is charging. Voltage at point A rises until point B becomes low and output high. C_1 then discharges until inverters change state again.



Low-frequency oscillator uses subharmonic sync

by Donald F. DeKold
Santa Fe Junior College, Gainesville, Fla.

A single-IC oscillator, which provides both sine-wave and square-wave outputs, can be synchronized with a submultiple (lower harmonic) of its output frequency. The circuit operates over a range of 1 to 500 kilohertz. Its applications include frequency multiplication, low-frequency filtering, and generation of low harmonics.

The oscillator requires a pulse or square-wave signal, whose frequency is f_o, from a low-impedance source. Capacitor C_1 and resistor R_1 differentiate the input into positive- and negative-going spikes. Diode D_1 couples only the negative spike to the inverting input (point A) of the comparator.

This forces the inverting input to be negative with respect to the non-inverting input. The comparator then switches, and point B becomes positive, creating a step voltage that is coupled by R_2 into the tank circuit formed by inductor L_1 and capacitor C_2.

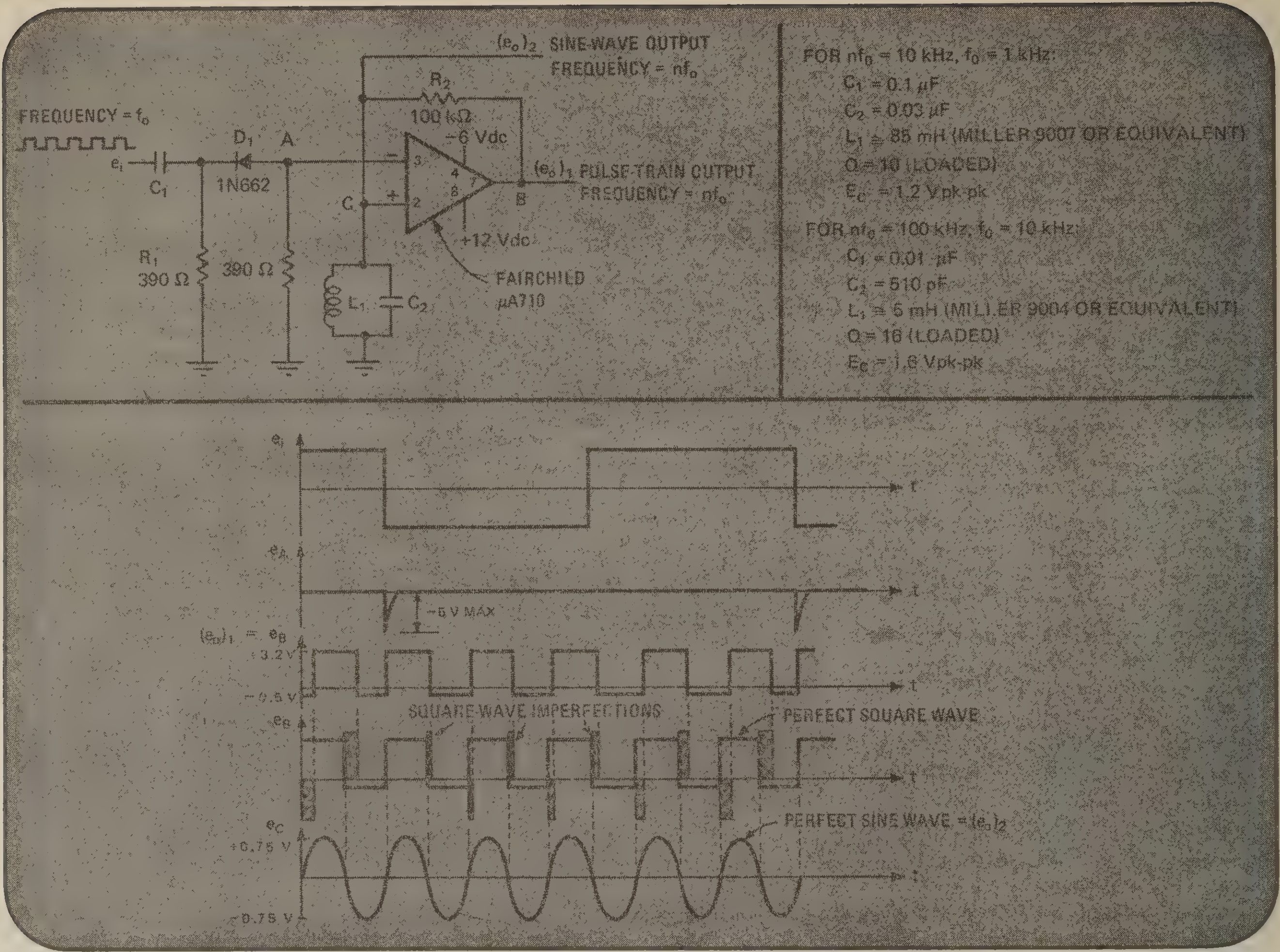
Every time the voltage across the tank crosses zero, the comparator switches. If the tank is excited by a positive step voltage, the initial voltage excursion of the ringing response across the tank will be positive. Similarly, if a negative-going step is applied, the excursion across the tank is negative.

Feeding back the output of the comparator to its input causes the positive and negative step voltages at point B continually to excite the tank. These steps form a square wave that is in phase with the ringing sinusoidal waveform at point C.

For stable synchronization, the oscillator frequency should be slightly less than nf_o, the desired output frequency. Each trailing edge of the input square wave becomes a synchronization pulse after differentiation.

The comparator output is forced to switch to its high value with the arrival of each new synchronization pulse prior to its free-run transition. It is then filtered by the LC circuit to yield a sine-wave output, which is taken from point C.

For the timing diagram shown, the pulse train at point B may be regarded as the superposition of a perfect square wave at frequency $5f_o$, in addition to a number of narrow pulses occurring at repetition rates of f_o.


(e₀)₂ SINE-WAVE OUTPUT FREQUENCY = nf₀
R₂
100 kΩ
−6 Vdc
FREQUENCY = f₀
D₁
A
eᵢ
C₁
1N662
(e₀)₁ PULSE-TRAIN OUTPUT FREQUENCY = nf₀
C
B
+12 Vdc
R₁
390 Ω
390 Ω
L₁
C₂
FAIRCHILD
µA710
FOR nf₀ = 10 kHz, f₀ = 1 kHz:
C₁ = 0.1 µF
C₂ = 0.03 µF
L₁ ≈ 85 mH (MILLER 9007 OR EQUIVALENT)
Q = 10 (LOADED)
E_C = 1.2 Vpk-pk
FOR nf₀ = 100 kHz, f₀ = 10 kHz:
C₁ = 0.01 µF
C₂ = 510 pF
L₁ ≈ 5 mH (MILLER 9004 OR EQUIVALENT)
Q = 16 (LOADED)
E_C = 1.6 Vpk-pk
eᵢ
t
e_A
−5 V MAX
(e₀)₁ = e_B
3.2 V
−0.5 V
SQUARE-WAVE IMPERFECTIONS
PERFECT SQUARE WAVE
e_B
PERFECT SINE WAVE = (e₀)₂
e_C
+0.75 V
−0.75 V

Signal locking. Oscillator keeps output signal in step with a subharmonic input. Differentiated trailing edge of input signal provides the synchronization pulse. Synchronized pulse train output from comparator is filtered by tank circuit to give synchronized sine-wave output. Comparator output is superposition of perfect square wave and narrow pulses that contain input harmonics.

The width of these narrow pulses depends on how much slower the comparator output is than the desired nf_o output. Since the narrow pulses are square-wave imperfections, they contain frequency components that are multiples of f_o.

A Fourier series analysis reveals that the amplitude of these components becomes smaller as their width decreases, or as oscillator frequency approaches nf_o. Since a square wave of frequency nf_o essentially is being filtered, even a moderate-Q tank circuit will result in practically perfect sine waves.

There are a few practical considerations that limit the oscillator's operating range. For output frequencies below 1 kHz, inductors may not be available with a high enough Q for good sine-wave outputs. Above 500 kHz, square-wave rise and fall times frequently increase to an objectionable degree.

For best performance, synchronization frequency ratios should range from 1 to 10. Although ratios as high as 40 can be obtained, the oscillator may lose its synchronization lock due to signal instabilities. Moreover, the synchronization pulse, which varies from −3 to −5 volts, should decay to zero in less than one-sixth the period of the output signal.

Feedback zeros dc level of diode gating circuit

by Roland J. Turner
RCA Corp., Moorestown, N.J.

Whenever a tracking filter is changed from its low-Q state to its high-Q memory state, gating transients and dc offsets during the gating interval may introduce errors to the stored information. A closed-loop balanced-diode-bridge gating circuit minimizes these errors by employing a degenerative feedback loop that automatically forces the dc level at the gate output to zero.

An open-loop circuit can also be used to perform the signal gating, but it requires an expensive integrated circuit quad diode and is not self-compensating. The success of this approach depends on maintaining each diode voltage drop within 5 millivolts, matching the diode leakage currents over temperature, and keeping diode capacitance low as well as matched.

With degenerative feedback, less expensive diodes can be used, and the gate dc output is self-correcting despite temperature variations. Cost for the entire gating circuit is less than \$5, instead of the \$25 or so for a circuit using the expensive matched diodes.

The block diagram shows a quad diode bridge embedded in a complementary control flip-flop. When a gating command (control pulse) is applied, the flip-flop becomes regenerative, changing the state of the gate. A degenerative control loop assures that the correction applied to half of the flip-flop forces the gate dc output to zero. A low-pass filter in the amplifier feedback path controls the speed at which the degenerative loop corrects for output dc offset errors. A detailed schematic illustrates the improved gating circuit.

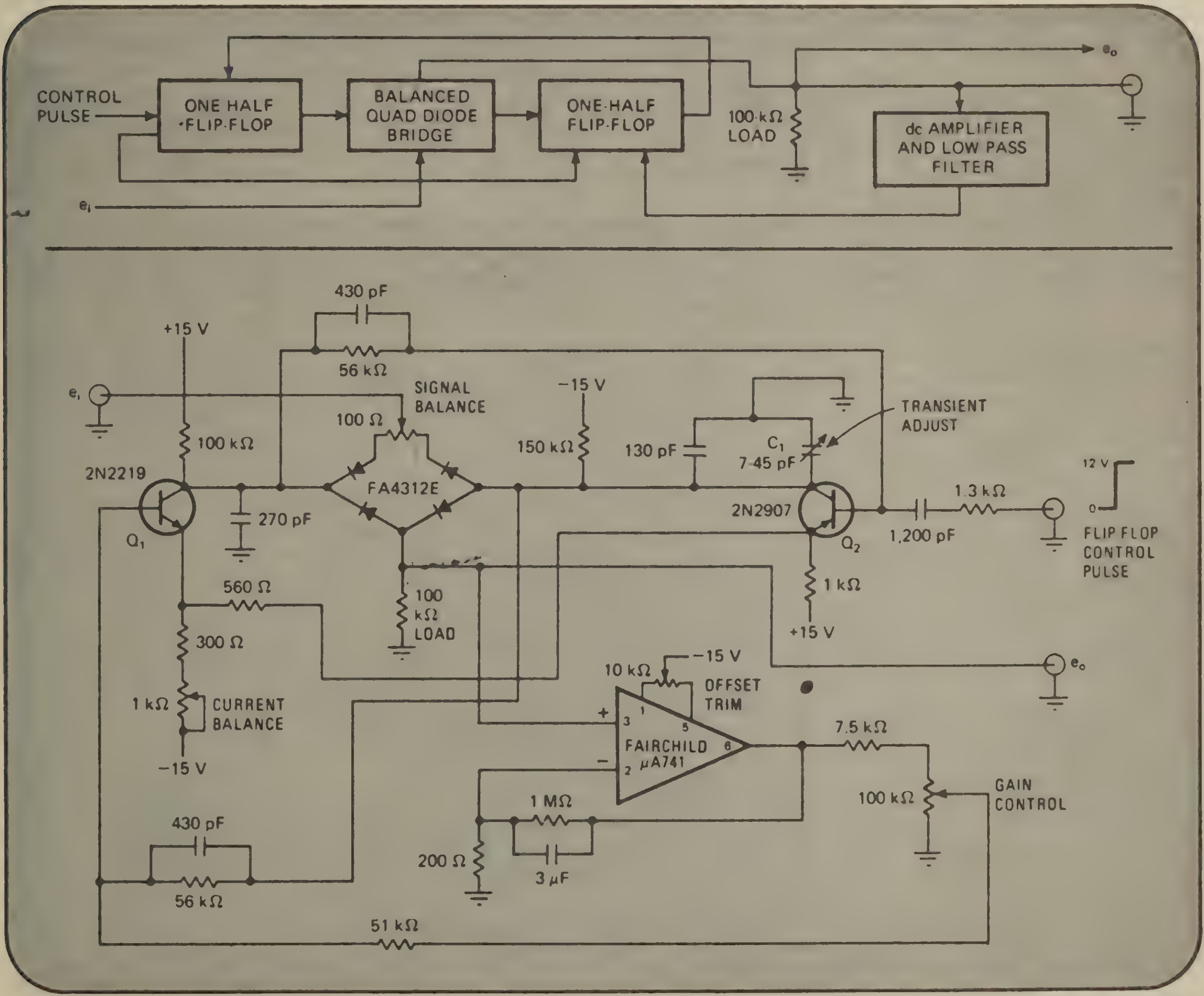
To stabilize dc signal level during the gate's off period, a differential operational amplifier compares the dc level at the output of the gate to ground reference. If the gate dc output is not zero, degenerative feedback to the base of Q_1 forces the dc signal level output of the diode bridge to zero. Transistor Q_1, which is the npn half of the complementary control flip-flop, actually cancels the dc signal that initiated the error.

Capacitor C_1 is adjustable to control the shape of the off-going voltage waveforms at the collectors of Q_1 and Q_2. This minimizes transient signal leakage into the gate's 100-kilohm output load. An actual measurement for transients across the load when the gate is turning off will yield a 10-microsecond pulse with a peak amplitude of 5 mV. If the gate is turning on, the transient is also a 10-μs pulse but with a 50-mV peak amplitude. When gating at high-impedance levels, the more critical transient is the off-going one.

The emitter loop of Q_1 contains a current balance potentiometer that corrects for any difference between the initial drive currents of Q_1 and Q_2. The signal balance adjustment in the diode bridge compensates for any bridge signal imbalance that may occur because the diodes are not precisely matched.

Instead of discrete transistors Q_1 and Q_2, the complementary flip-flop can be realized with an integrated circuit—Motorola's type MD6003.

Low-transient gate. Differential amplifier monitors output of diode bridge, which is flanked by complementary control flip-flop. The dc output signal, if other than zero, is automatically forced to zero by the degenerative feedback of Q_1. Transients across 100-kilohm load are minimized during the off-going state of the gate. Feedback assures stable operation over a wide temperature range.



Resistance change alters filter's output function

by Frank Vitaljic
Bellingham, Wash.

A variable-function filter can be made with an active RC network by simply changing the value of a single resistor. For specific values of a feedback resistor, R_f in circuit (a), either all-pass, bandpass, or notch filter functions can be implemented.

Network filtering function is variable since the circuit's two zeros are movable, while its two poles remain fixed. Values of R_f that lie between the points where the filtering function changes cause a linear variation in the circuit's voltage amplitude ratio at the center frequency, $\omega^{\Sigma\infty o}$.

If R_f is some high value, a pole-zero plot (b) shows that the zeros are located on the positive and negative imaginary axes, resulting in a notch filter. As R_f is decreased, the zeros travel on a circular path towards each other. When they are diametrically opposite the network poles, an all-pass filter is realized.

Further decreasing R_f causes the zeros to coincide on the real axis, where they split and then travel in opposite directions—one towards the origin, and the other towards infinity. When R_f is reduced to zero, a bandpass filter results with one zero at the origin and the second at infinity.

Examining the network's transfer function will illustrate circuit action. The basic circuit (a) has an all-pass transfer function:

$E_2/E_1 = k\,D(-s)/D(s)$

where k is a constant, s the Laplace transform variable, and:

$D(s) = s^2 + \omega_o s/Q + \omega_o^2$

and $D(-s) = s^2 - \omega_o s/Q + \omega_o^2$

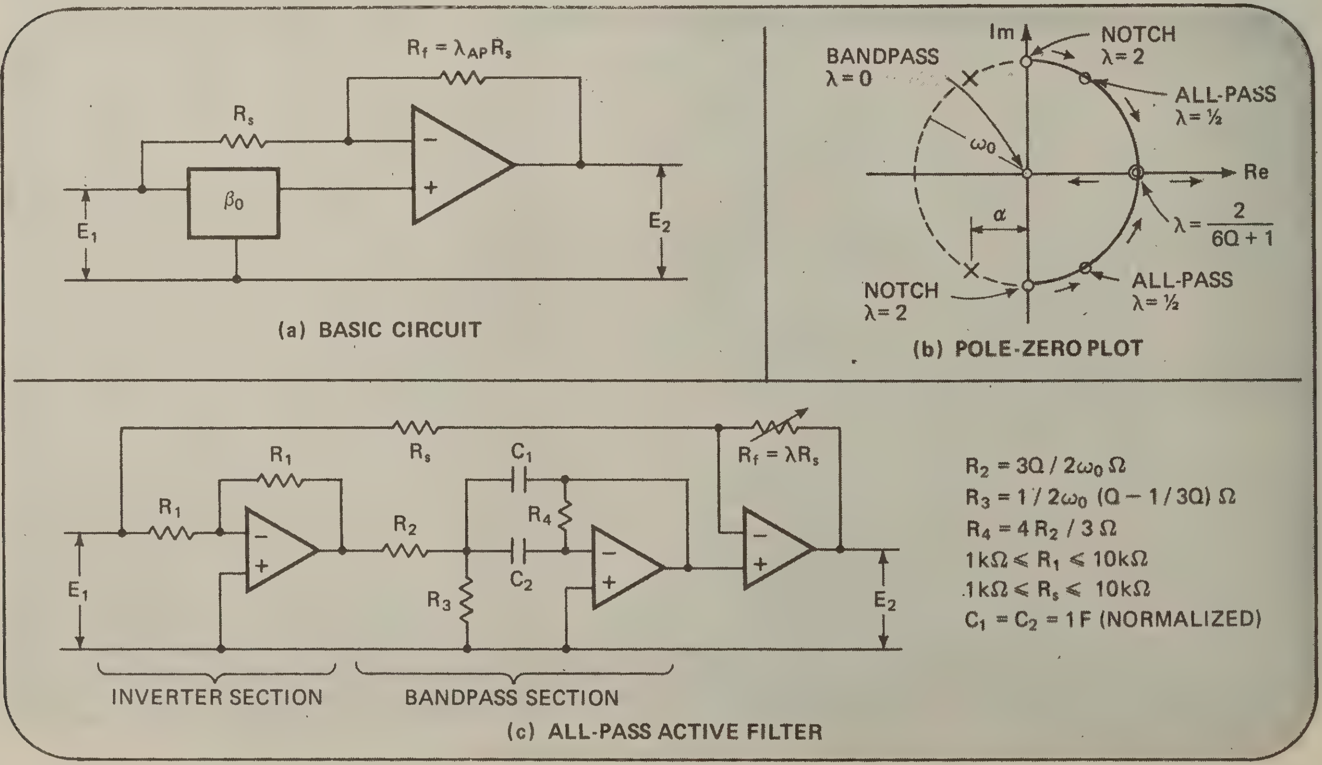
where $Q = \omega_o/2\alpha$

and α is the real part of the complex pole pair (as shown in the diagram).

The network represented by $\beta^{\Sigma\infty o}$ is actually a bandpass filter. The value of R_f needed to realize an all-pass function is denoted by $\lambda_{AP}R_s$. If $k \neq\_ +1$, then either bandpass or notch filters can be implemented by adjusting λ.

For example, when $k = -\lambda^{\Sigma\infty AP}$, the $\beta^{\Sigma\infty o}$ network is a bandpass filter:

Variable active filter. Decreasing the resistance of feedback resistor, R_f, changes filtering action of basic active circuit (a) from notch to all-pass to bandpass network. As shown in (b), poles of transfer function are fixed, but zeros move toward real axis, where they meet and then split. When R_f is zero, one zero is at the origin, the other is at infinity. Actual all-pass filter (c) requires three differential amplifiers.



(a) BASIC CIRCUIT

(b) POLE-ZERO PLOT

(c) ALL-PASS ACTIVE FILTER

$$\beta_o = \frac{\lambda_{AP}}{1 + \lambda_{AP}}\left[\frac{D(s) - D(-s)}{D(s)}\right]$$

$$\beta_o = \frac{2\omega_o\lambda_{AP}}{Q(1 + \lambda_{AP})}\left[\frac{s}{s^2 + \omega_o s/Q + \omega_o^2}\right]$$

The overall circuit transfer function becomes:

$$\frac{E_2}{E_1} = \frac{\lambda_{AP}}{1 + \lambda_{AP}}\left[\frac{\lambda_{AP} - \lambda}{\lambda_{AP}} - \frac{(1 + \lambda)D(-s)}{D(s)}\right]$$

An all-pass filter results when $\lambda = \lambda^{\Sigma\infty AP}$:

$$\frac{E_2}{E_1} = \frac{\lambda_{AP}}{1 + \lambda_{AP}}\left[\frac{\lambda_{AP} - \lambda_{AP}}{\lambda_{AP}} - \frac{(1 + \lambda_{AP})D(-s)}{D(s)}\right]$$

$$\frac{E_2}{E_1} = \lambda_{AP}\left[-\frac{D(-s)}{D(s)}\right]$$

Since $k = -\lambda^{\Sigma\infty AP}$, then:

$E_2/E_1 = k\,D(-s)/D(s)$

which is the original all-pass circuit transfer function.

Similarly, when $\lambda = 0$, a bandpass filter is realized:

$$\frac{E_2}{E_1} = \frac{\lambda_{AP}}{1 + \lambda_{AP}}\left[\frac{\lambda_{AP}}{\lambda_{AP}} - \frac{D(-s)}{D(s)}\right]$$

$$\frac{E_2}{E_1} = \frac{\lambda_{AP}}{1 + \lambda_{AP}}\left[\frac{D(s) - D(-s)}{D(s)}\right]$$

And when $\lambda = 2\lambda^{\Sigma\infty AP}/(1-\lambda^{\Sigma\infty AP})$, the circuit is a notch filter:

$$\frac{E_2}{E_1} = \frac{\lambda_{AP}}{1 + \lambda_{AP}}\left[\frac{\lambda_{AP} - 2\lambda_{AP}/(1 - \lambda_{AP})}{\lambda_{AP}} - \left(1 + \frac{2\lambda_{AP}}{1 - \lambda_{AP}}\right)\frac{D(-s)}{D(s)}\right]$$

$$\frac{E_2}{E_1} = \frac{\lambda_{AP}}{1 + \lambda_{AP}}\left[\frac{(1-\lambda_{AP})D(s) - 2D(s) - (1+\lambda_{AP})D(-s)}{(1-\lambda_{AP})D(s)}\right]$$

An actual all-pass circuit is shown in (c) for $\lambda^{\Sigma\infty AP} = -k = ½$. The resistor values are scaled with respect to the capacitors.

Triggered sweep generator responds to 100-ns spike

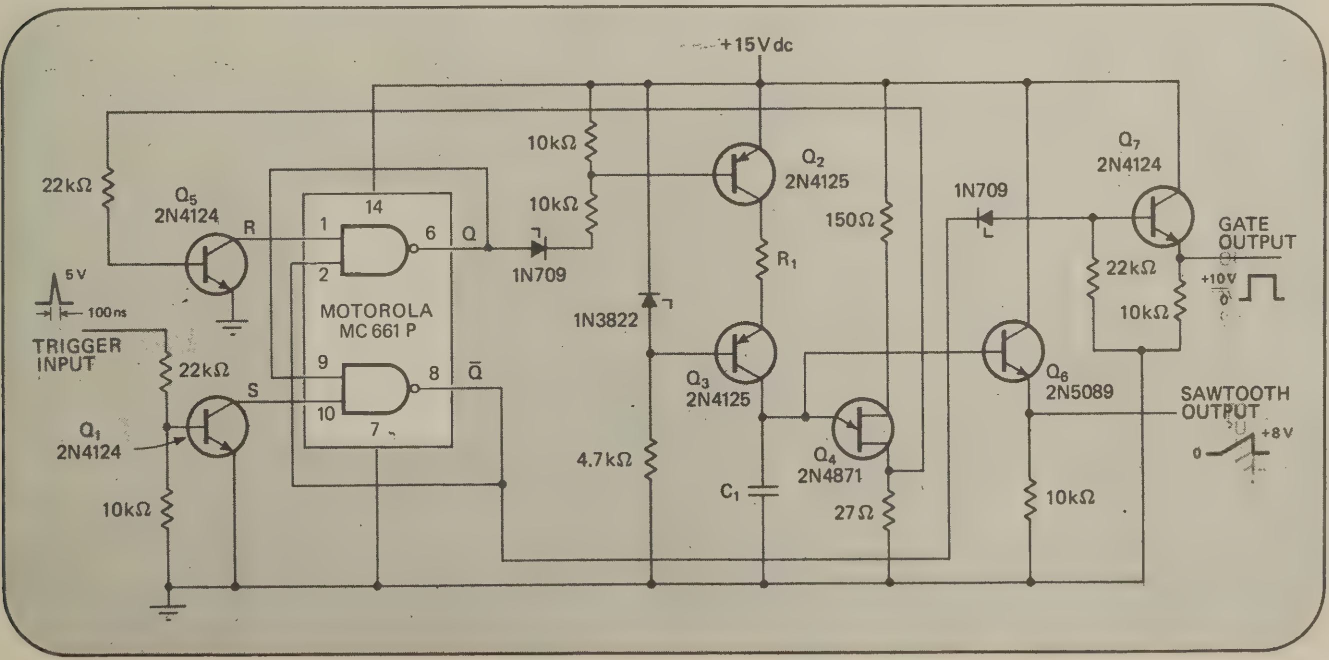
by Lawrence Sperling
Monroeville, Pa.

Connecting a dual high-threshold-logic (HTL) NAND gate as a set-reset flip-flop gives a triggered sweep generator that provides a 2%-linear ramp when triggered with a 5-volt 100-nanosecond pulse. Sweep speeds for the circuit range from 10 seconds down to 10 microseconds. Moreover, duty cycle for a second output, a gating pulse, can be as high as 95%.

When the flip-flop is set with a trigger pulse through transistor Q_1, its Q output goes low, allowing transistor Q_2 to saturate. Since Q_2 is conducting, transistors Q_3 and Q_4 generate a ramp output, the timing of which is controlled by capacitor C_1.

A constant current, determined by resistor R_1 and the voltage across it, charges capacitor C_1. The resistor's voltage (V_{R1}) for the sawtooth output shown is approxi-

Flip-flop trigger. Bistable formed by dual NAND gate accepts high-speed trigger pulse for sweep generator circuit. Input spike sets bistable, its Q output goes low, Q_2 saturates, and C_1 charges. When voltage across C_1 reaches threshold of UJT Q_4, the transistor fires, discharging C_1, which applies a pulse to Q_5 that resets the bistable. The sweep generator is now ready to be triggered again.



mately 3 v for the generator in the diagram.

Capacitor C_1 charges until the voltage across it reaches the triggering point of unijunction transistor Q_4. When Q_4 turns on, C_1 discharges and a positive pulse is applied to the base of Q_5. This resets the flip-flop to its normal state, with the Q output high. The sweep generator can now accept a new trigger pulse.

Output sweep voltage is buffered through Q_6 so that a load will have a negligible effect on sweep length. This emitter-follower introduces a slight output delay, for which the circuit can be compensated. In addition to providing a sawtooth output, the circuit offers a gate output, which is taken from the flip-flop's Q output and buffered through transistor Q_7.

It is simple to find the timing for sweep speed:

$t = C_1V_o/I_{R1}$

where V_o is the maximum output sweep voltage, and I_{R1} the current through R_1. Since $I_{R1} = V_{R1}/R_1$, then:

$t = R_1C_1V_o/V_{R1}$

Output voltage, V_o, is determined by the product of Q_4's intrinsic stand-off ratio (η) and its interbase voltage (V_{BB}). For this particular UJT, ηV_{BB}, equals 8 v. Therefore:

$t = 8\,R_1C_1/V_{R1}$

Values for resistor R_1 should range between 100 ohms and 100 kilohms. Values for capacitor C_1 depend primarily on the resistance selected for R_1; the suggested low limit is 1,000 picofarads.

Broadband pulse generator uses small timing capacitance

by Ron Siebert
Signetics Corp., Sunnyvale, Calif.

An inexpensive, widerange pulse generator keeps capacitor values low, even at operating frequencies down to 0.3 hertz. Instead of large capacitances, the circuit uses a field effect transistor and a high-value variable timing resistor to give large time constants.

The generator, which operates from 0.3 Hz to more than 10 megahertz, consists of only one integrated circuit, a FET, two resistors, and one capacitor. It has no special power requirements, and operates over a supply range of 4 to 6 volts.

The FET performs as a source-follower; and because of its high input impedance, the timing resistor, R_1, can be quite large. This allows the timing capacitor, C_1, to become small for a particular output frequency.

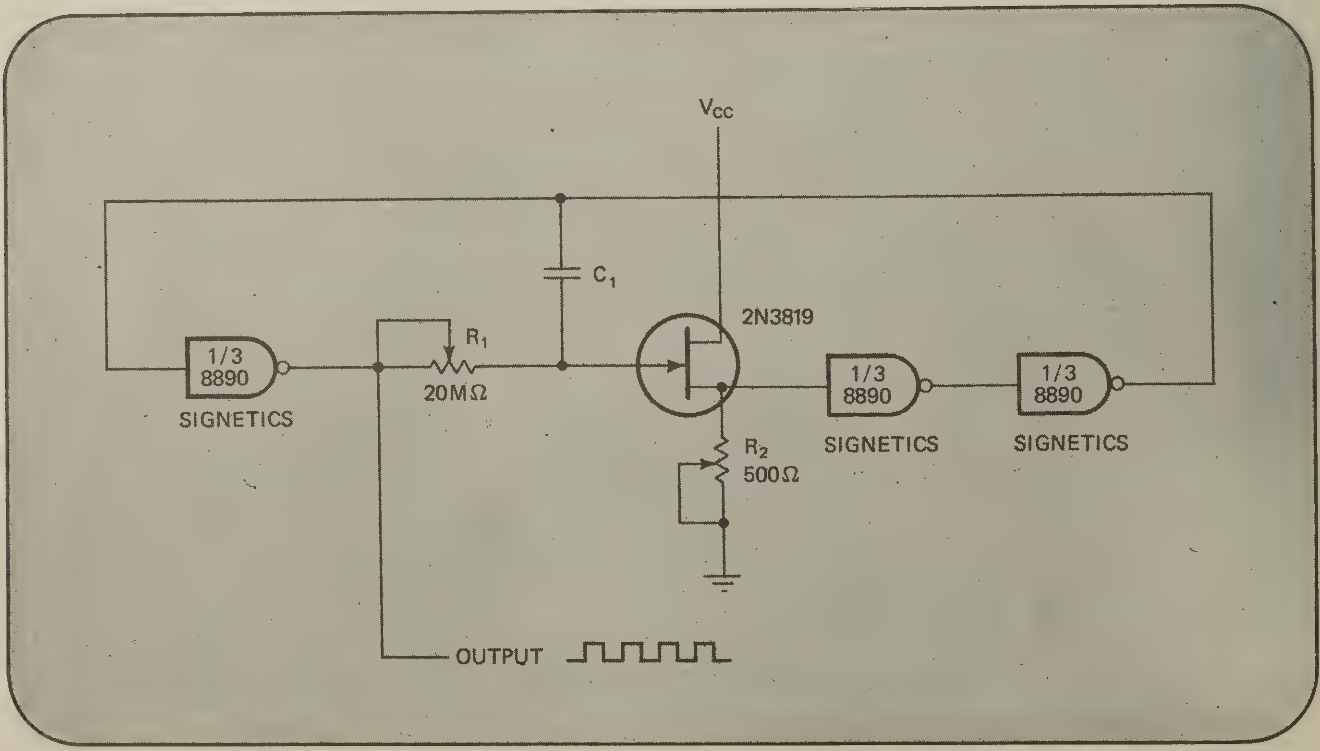
Three TTL NAND gates provide the gain and regenerative feedback needed to sustain circuit oscillation. The generator's output is a pulse train the duty cycle of which can be adjusted with potentiometer R_2.

Frequencies as low as 0.3 Hz can be obtained when C_1 is as small as 0.1 microfarad. Timing resistor, R_1, may be varied from a few hundred ohms to 20 megohms, resulting in a frequency change for the output of over 50,000:1.

To calculate the output frequency (f_o) for specific values of R_1 and C_1, let:

$f_o = \frac{1}{2}R_1C_1$

High R, low C. Generator can deliver 0.3-hertz pulse output with timing capacitor as small as 0.1 microfarad. High input impedance of FET and large timing resistance keep time constant large.



Light-emitting diode pair forms null indicator

by Michael H. Loughnane
Temple University, School of Medicine, Philadelphia, Pa.

Visual indication of a null voltage to ±0.2 millivolt can easily be accomplished by using light-emitting diodes in the feedback loop of an operational amplifier. When both LEDs are dark, the input voltage is approximately 0, indicating a null.

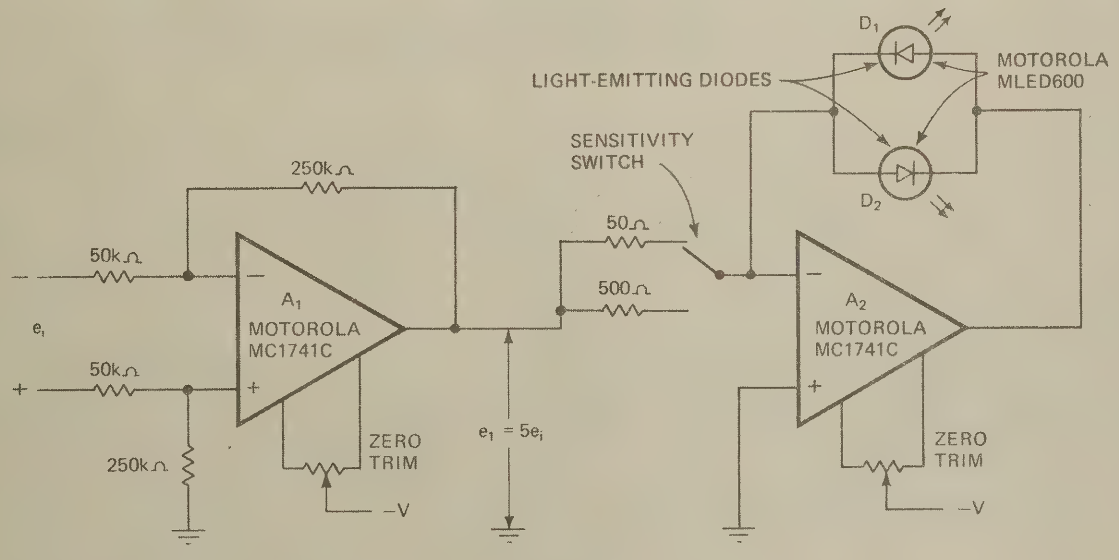
Differential amplifier A_1 provides a single-ended, low-impedance output for driving A_2, which functions as a zero-crossing detector. When A_2's output is between ±1.4 V (the forward-voltage drop of the LEDs), the amplifier operates with essentially open-loop gain.

With a negative input voltage (e_1 less than 0 V) applied to A_2, only diode D_1 conducts (lights); with a positive input (e_1 greater than 0 V), only D_2 will light. As e_1 approaches 0 V (null), the current through the conducting diode decreases and both LEDs appear dark, even though one is really in a clamped state.

Both brightness and width of the null band are controlled by the sensitivity switch. When 500 ohms is selected, the input voltage can be nulled with a repeatability of about ±2 mV in ambient light. Switching to 50 ohms improves repeatability to ±0.2 mV. Even better sensitivity can be achieved if the LEDs are shielded from ambient light.

Total parts cost is approximately $10. The trimmers allow amplifier offset voltage to be zeroed out.

LED null indicator. Two-amplifier circuit uses light-emitting diodes to pinpoint null voltages within ±0.2 mv under normal lighting conditions. Amplifier A_1 supplies proper driving signal for zero-crossing detector A_2. For negative inputs to A_2, D_1 lights; for positive inputs, D_2 lights. When a null is reached both LEDs are dark. Measurement sensitivity depends on position of switch at input of A_2.



VISUAL INDICATION

	$e_i > 0$V	$e_i < 0$V	$e_i \approx 0$V
D_1	●	●	●
D_2	●	●	●

NULL SENSITIVITY

SWITCH RESISTANCE	NULL ACCURACY
50 OHMS	± 0.2 mV
500 OHMS	± 2 mV

Widerange multivibrator costs just 25¢ to build

by Michael Faiman
University of Illinois, Urbana, Ill.

A simple astable multivibrator can be made from one-half an inexpensive integrated circuit, a load resistor, and a single timing capacitor—bringing total parts cost to about 25 cents. The circuit (a) never fails to start and can generate frequencies from under 1 hertz to over several megahertz. Its on-to-off-time ratio is almost unity and is unaffected by the value of the capacitor.

The multivibrator employs a TTL hex inverter with open-collector outputs (a type 7405, for example). To understand circuit operation, look inside the integrated circuit: (b) shows Q_1 as the output transistor of inverter I_1 and Q_2 as the input transistor of inverter I_2.

Suppose that node b is low so that node c is high, Q_1 is in saturation, and node a is clamped at V_{SAT} (about 0.2 volt). The voltage at node b rises exponentially towards $V_{CC} - V_{BE}$ with the time constant R_1C. When node b reaches the threshold voltage (V_T, about 1.4 V) required to switch Q_2, node c goes low, turning off Q_1.

Current through R_2, which was flowing into Q_1 via the emitter of Q_3, can now pass only into the base of Q_4 and the left side of capacitor C. Transistors Q_4 and Q_5 turn on, causing the voltage at node a to jump to V_T. This voltage step is transmitted through the capacitor to node b, which rises to the potential $2V_T - V_{SAT}$.

Transistors Q_3, Q_4, and Q_5 now behave like an operational amplifier. Although Q_4 and Q_5 are on, they are not saturated. Aside from a small base current into Q_4, most of the current through R_2 flows into C and Q_5 via the emitter of Q_3.

If this current increases, the voltage at node a drops, reducing the base drive at Q_4, which tends to turn off both Q_4 and Q_5. Since less current can pass from C into Q_5, the voltage at node a goes up. A similar process occurs if the voltage at node a rises, since it is clamped at V_T by negative feedback through capacitor C.

The capacitor receives a constant current from R_2, which causes the voltage at node b to fall linearly. When it reaches V_T, Q_2 switches back to its former state, node c goes high, and Q_1 saturates. Also, the voltage at nodes a and b snaps back down to V_{SAT}, and the cycle is complete. The node waveforms are shown in (c).

Circuit on time (t_{on}) and off time (t_{off}) are easily obtained by neglecting the switching times of the individual transistors and Q_4's base current when it is on:

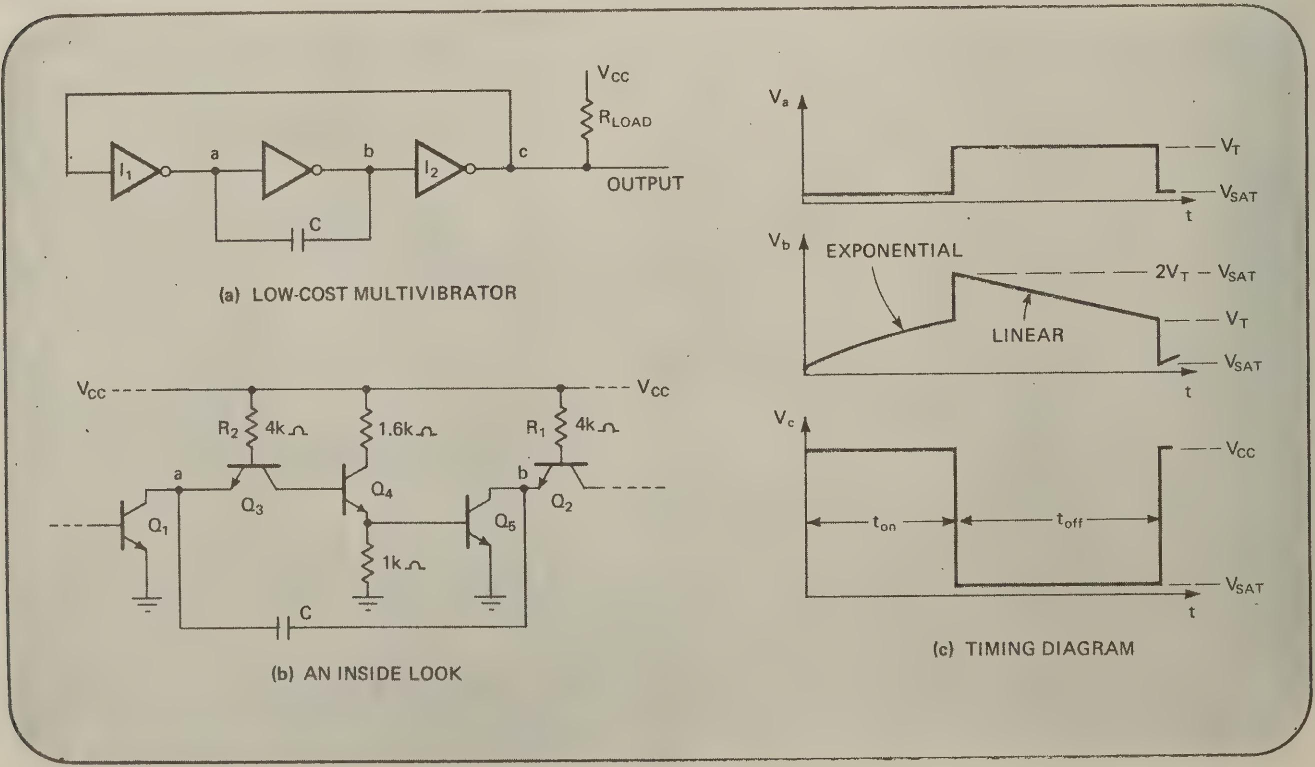
$$t_{on} = R_1C \ln [(V_{CC}-V_{BE}-V_{SAT})/(V_{CC}-V_{BE}-V_T)]$$

$$t_{off} = R_2C(V_T-V_{SAT})/(V_{CC}-V_{BE}-V_T)$$

Nominal circuit values of $R_1 = R_2$, $V_{CC} = 5$ V, $V_{BE} \doteq 0.8$ V, $V_{SAT} = 0.2$ V, and $V_T = 1.4$ V yield an on-to-off-time ratio of t_{on} st_{off} approximately equals 0.83 or 5/6.

If equal on and off times are needed, t_{off} may be reduced, without affecting t_{on}, by connecting a suitable resistor (about 26 kilohms when $R_1 = R_2 = 4$ kilohms) between node a and V_{CC}. Capacitor values range from 300 microfarads to 300 picofarads for output frequencies from 1 Hz to 1 MHz.

Inexpensive multi. Three inverters, a resistor, and a capacitor make up this 25-cent multivibrator. With Q_1 saturated, node b is low and node c is high. Voltage at b then increases exponentially until Q_2 switches, so that node c goes low and Q_1 turns off. R_2 then delivers constant current to capacitor C, making voltage at b decrease linearly until Q_2 switches again. Node c is now high and Q_1 saturated.


(a) LOW-COST MULTIVIBRATOR

(b) AN INSIDE LOOK

(c) TIMING DIAGRAM

IC frequency doubler runs at logic speed

by C.H. Doeller III and Aaron Mall
Bendix Corp., Baltimore, Md.

Two integrated circuits can serve as a digital frequency doubler that can perform at the operating frequency of the logic used. The frequency range of conventional doublers usually is limited to about one decade because they use discrete resistors and capacitors. But the circuit shown successfully operates at frequencies as high as 10 megahertz over a temperature range of –55°C to +125°C.

When the input signal is at ground potential, the outputs of NAND gates G_1 and G_2 are positive, and the output of NOR gate G_3 is grounded. If the input signal transition is positive, the output of G_1 goes low and forces G_3's output to become high a gate delay later.

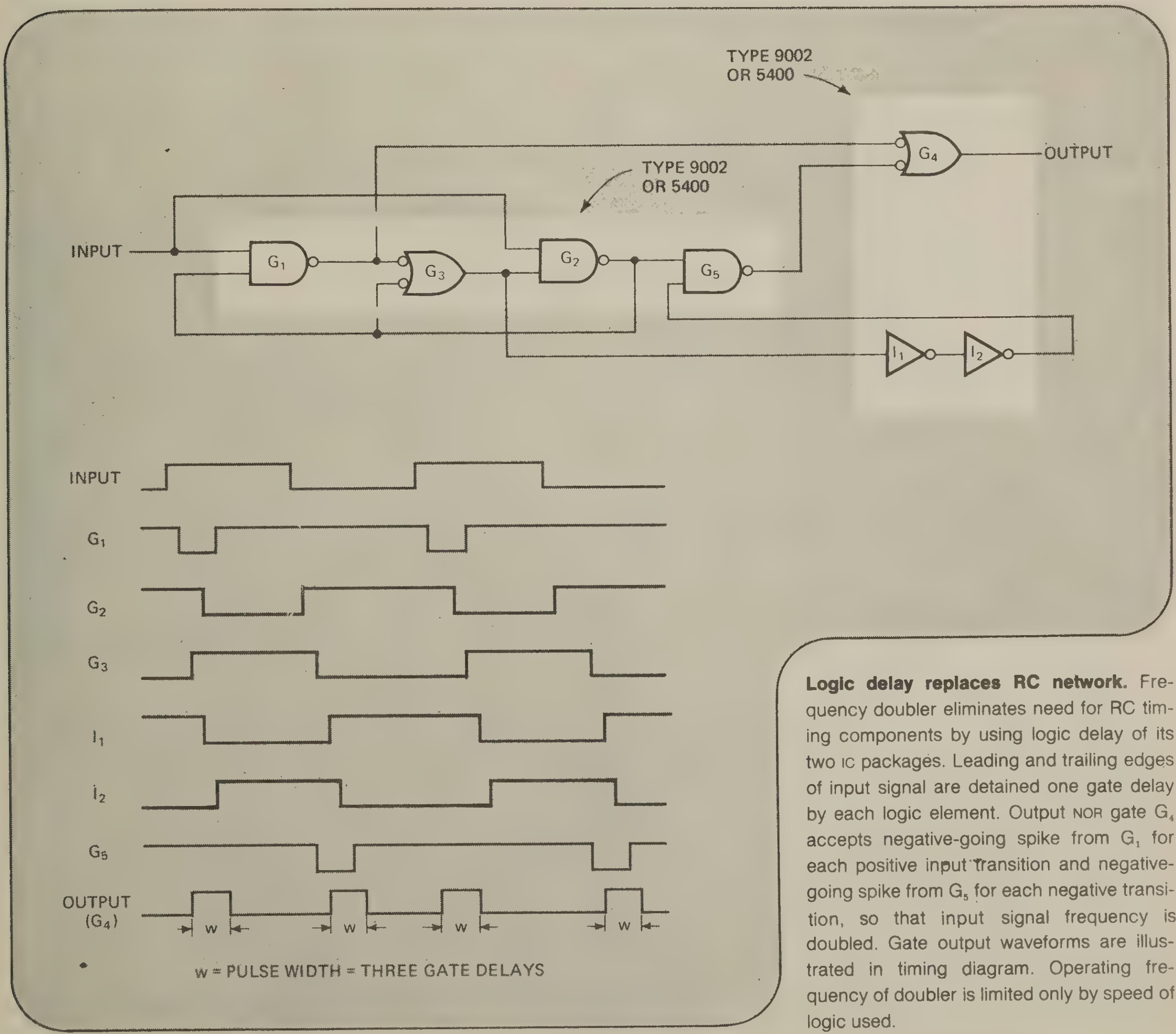
With two positive inputs to G_2, its output goes to ground. The output of G_1 becomes positive, resulting in a sharp negative-going pulse that is applied to output NOR gate G_4. Circuit output is a positive-going spike.

Gate G_3 follows the input signal and drives inverters I_1 and I_2. These delay the input-pulse trailing edges by the same gate delay as the leading (positive) edges.

The output of G_2 is an inverted, delayed version of the input signal that is applied to NAND gate G_5 along with the output of I_2. This causes G_5 to produce a negative-going pulse at every negative transition of the input signal.

Because the output of G_5 is applied to output NOR gate G_4, there is a positive-going output pulse at every negative transition of the input pulse train. Input signal frequency is doubled since G_1 contributes a sharp pulse for every leading edge of the input, while G_5 gives an identical pulse for every trailing edge.

Symmetry of the doubled signal is affected only by the symmetry of the input waveform. The timing diagram shows the output waveform for each gate.



w = PULSE WIDTH = THREE GATE DELAYS

Logic delay replaces RC network. Frequency doubler eliminates need for RC timing components by using logic delay of its two IC packages. Leading and trailing edges of input signal are detained one gate delay by each logic element. Output NOR gate G_4 accepts negative-going spike from G_1 for each positive input transition and negative-going spike from G_5 for each negative transition, so that input signal frequency is doubled. Gate output waveforms are illustrated in timing diagram. Operating frequency of doubler is limited only by speed of logic used.

Fast ECL-to-TTL interface shifts data for 80¢ per bit

by R.R. Osborn
New York, N.Y.

A single integrated circuit, a few resistors, and one capacitor are all that's needed to build an ECL-to-TTL interface that operates at the speed of emitter-coupled logic—and total component cost is only about 80¢ per bit. Normally, converting the 0.8-volt swing of ECL to the 2-V swing needed for transistor-transistor logic requires at least four active devices for amplification and level shifting. Commercially available interfaces operate with a delay of about 19 nanoseconds and cost approximately $1.60 per bit.

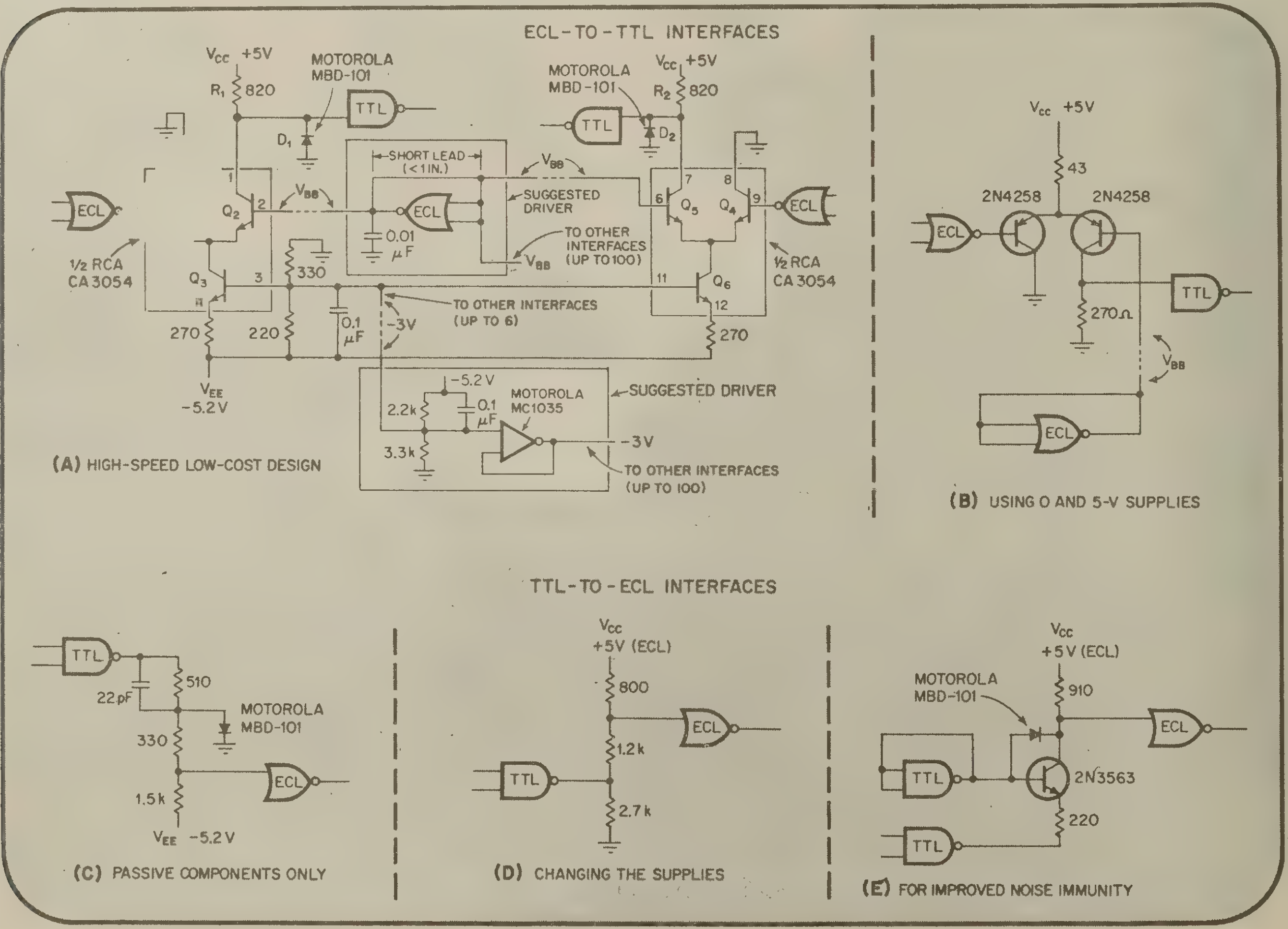
The circuit of (A) allows ECL to be used wherever its high-speed performance is most advantageous; the TTL takes over for all other functions where its low cost and ready availability are beneficial. The interface, which operates in the emitter-coupled mode, employs hot-carrier diodes D_1 and D_2 to prevent transistor saturation. This eliminates transistor storage time so that the circuit performs at ECL speed.

Transistors Q_1 and Q_2 act as switches, while Q_3 is a constant-current source. With a high ECL signal present, Q_1 is on and Q_2 is off. The constant current from Q_3 is directed to ground by Q_1, and resistor R_1 pulls Q_2's collector to the supply potential (5 V in this case).

When a low ECL input is applied, Q_1 turns off and Q_2 turns on. Q_2 then switches the constant current to R_1 and the TTL gate. Diode D_1 prevents Q_2 from saturating by clamping the collector to –0.7 V. (D_1 can be eliminated if the TTL gate has an input clamping diode.)

The operation of the right-hand side of the circuit is

Logic shifting. Circuit (A) translates 0.8-volt ECL data to 2-V TTL data at the speed of ECL. Q_1 and Q_2 switch constant current of Q_3. With Q_1 off, Q_2 switches Q_3's current to R_1 and the TTL gate. Q_2 cannot saturate because of D_1 clamp, thus eliminating transistor storage time and increasing operating speed. Interface (B) offers alternate supply arrangement. Circuits (C), (D) and (E) are TTL-to-ECL interfaces.



(A) HIGH-SPEED LOW-COST DESIGN

(B) USING 0 AND 5-V SUPPLIES

(C) PASSIVE COMPONENTS ONLY

(D) CHANGING THE SUPPLIES

(E) FOR IMPROVED NOISE IMMUNITY

identical. With a high ECL input, Q_4 conducts, Q_5 is off with its collector tied to 5 V through R_2, and Q_6's constant current is grounded. With a low ECL signal present, Q_4 switches off, and Q_5 carries the constant current of Q_6 to R_2 and the TTL gate. Diode D_2 stops Q_5 from going into saturation.

Two recommended driver configurations also are illustrated. Each one can be used for as many as 100 additional interface circuits. Therefore, the number of ECL-to-TTL conversions easily can be extended to 100 data bits.

Usually, an ECL gate is powered with supply voltages of $V_{EE} = -5.2$ V and $V_{CC} = 0$ V. If it is necessary to use $V_{EE} = 0$ V and $V_{CC} = 5$ V, the interface of (B) can be employed, though two precautions must be observed: the ECL gate must be carefully decoupled from any TTL noise on the 5-V power line, and the V_{CC} supply must be a low-impedance quiet source to counter a 0-decibel noise rejection from the positive supply to the logic outputs.

Diagrams (C), (D) and (E) show suggested TTL-to-ECL interfaces. Circuit (C) uses only passive components; its 22-picofarad capacitor can be omitted if stray capacitance is low or if high speed is not essential. The diode provides a 0.7-V reference when the TTL input is high.

Both (D) and (E) employ a 5-V supply as the V_{CC} voltage for the ECL gate. Circuit (E) is recommended for improved noise-immunity performance due to the high collector impedance of the transistor, which functions as a ground-base amplifier. The TTL gate that is coupled back on itself provides a TTL threshold level. As with circuit (A), the hot-carrier diode prevents the transistor from saturating, thereby improving speed.

Tunable active filter maintains constant Q

by Roger Melen
Stanford University, Palo Alto, Calif.

With a potentiometer at each end of a three-stage, state-variable filter's middle section, the resonant frequency of the circuit can be tuned without significantly altering circuit Q. The active bandpass filter shown has a Q of about 30 and a resonant frequency that can range from 150 to 1,500 hertz with a Q variation of less than 5%.

Leaving the dual potentiometer aside simplifies calculating the filter's resonant frequency (f_o) and bandwidth (B):

$$f_o = \tfrac{1}{2}\pi R_1C_1 = \tfrac{1}{2}\pi R_2C_2$$

and $B = \tfrac{1}{2}\pi R_3C_1$

where $R_1 = R_2$, and $C_1 = C_2$. The gain (A) and Q of the filter are equal since $Q = f_o/B$:

$$A = Q = R_3/R$$

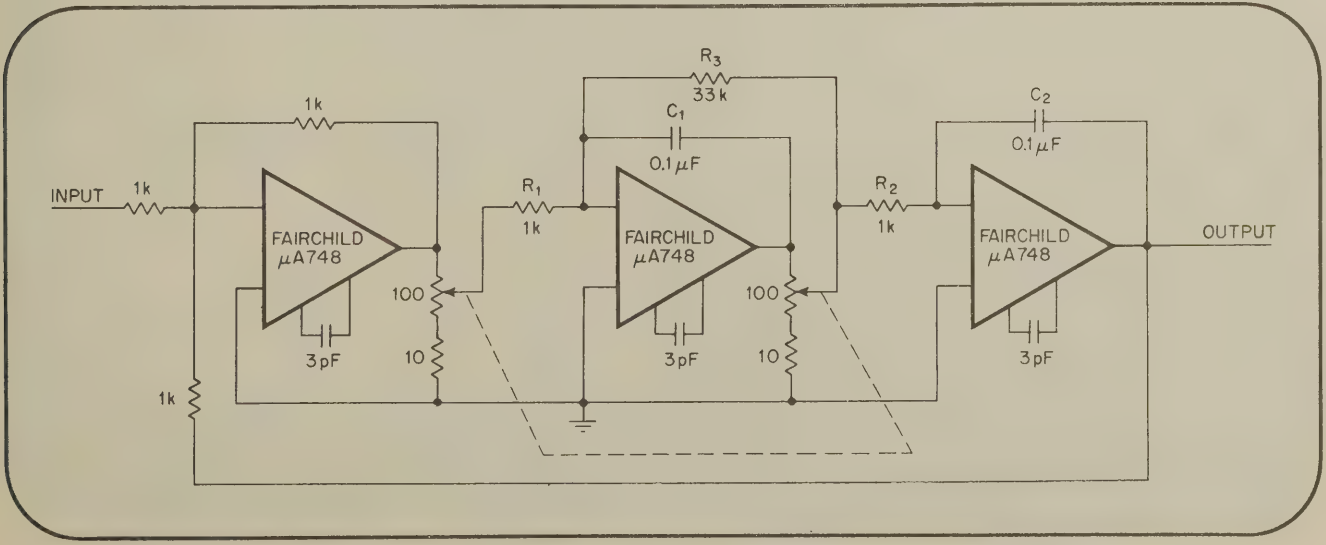
where $R = R_1 = R_2$.

Putting the potentiometer in the circuit just adds a voltage divider that decreases current flow through R_1, R_2, and R_3. The smaller current causes an apparent simultaneous increase in the values of these resistors.

As the potentiometer setting is varied, both the filter bandwidth and resonant frequency are tuned. However, circuit Q remains approximately constant because both R and R_3 change in the same direction and with the same proportional magnitude.

The filter's operating frequency range can be shifted by changing the capacitors. The tunable bandwidth, however, will not be appreciably altered unless the potentiometer and the two 10-ohm resistors also are different. Uses include signal recovery tasks.

Potting down Q. Depending on setting of dual potentiometer, tunable filter can resonate anywhere within a frequency decade (from 150 to 1,500 hertz) with little change in circuit Q or gain. Potentiometer divides interstage voltage so that current through R_1, R_2 and R_3 drops, simulating proportionate resistance increases. Resonant frequency shifts but Q remains constant (less than 5% variation).



Detector measures phase over full 360° range

by Charles A. Herbst
Fort Lee, N.J.

Because it halves the phase difference between two input signals, a digital differential phase meter can perform measurements over a full 360° range. Moreover, the circuit is easy to build and calibrate.

The circuit detects the average phase (time) difference between any two sine, square, triangle, or pulse inputs with the same frequency. It can handle frequencies from 100 hertz to beyond 1 megahertz over an amplitude range of about 0.5 to 10 volts peak-to-peak. Total parts cost is low since only five IC packages are needed.

One input signal, e_a, acts as a reference, while the other, e_b, is the test signal from the network under measurement. Both signals are clipped and squared by comparators A_1 and A_2, resulting in logic-level pulses that are buffered and inverted before being applied to flip-flops FF_1 and FF_2.

The flip-flops perform as binary counters, dividing the input frequency by two so that the phase difference between e_a and e_b also is divided by two. This division extends the measurement range of the circuit from 180° to 360° (since the four-gate exclusive-OR phase comparator sees 90° rather than 180°, or 45° instead of 90°).

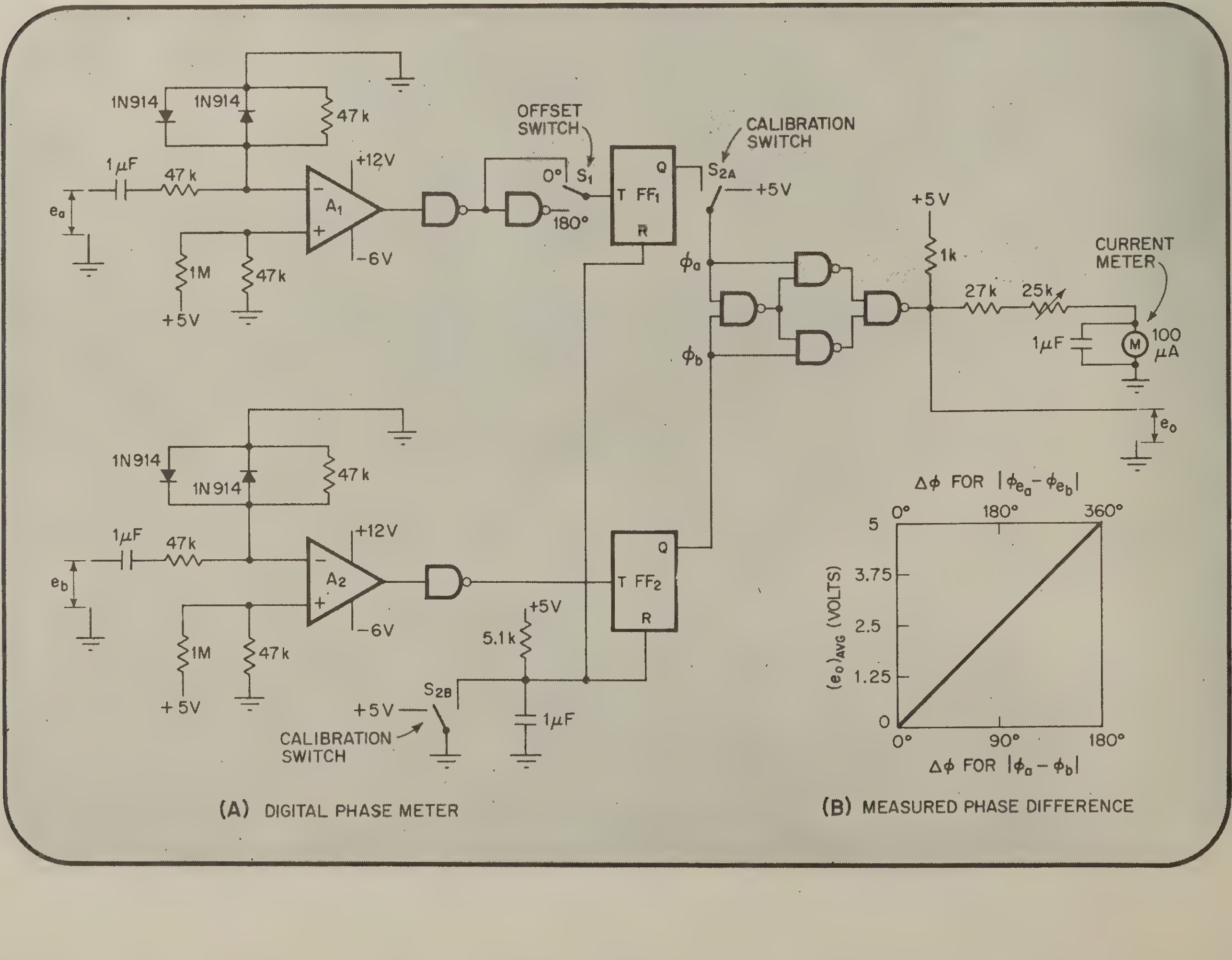
Any phase difference between the outputs of FF_1 and FF_2 is converted into a train of width-modulated pulses by the digital phase comparator. These pulses then are time-averaged into an analog current by the low-pass filtering action of the meter circuit. The value of the analog current represents the phase difference between e_a and e_b.

With a divide-by-two counter, the circuit can measure phase differences up to 360°. Using a divide-by-four counter would extend the circuit's measuring range to 720°, but at the expense of resolution and accuracy.

The offset switch, S_1, creates a midscale zero-phase position on the meter so that the initial direction of the relative phase shift of the network under test can be determined. The calibration switch, S_2, sets the flip-flops to zero and applies noncoincident inputs to the exclusive-OR phase detector during a full-scale meter calibration check.

This digital phase meter uses TTL integrated circuits: two type 710 comparators, two type 7400 NAND gate packages, and one Texas Instruments SN7473 dual flip-flop. The circuit also employs an ammeter with a full-scale deflection of 100 microamperes.

Measuring phase. Comparators A_1 and A_2 clip and square inputs e_a and e_b. After being buffered and inverted, the signals then are halved by flip-flops FF_1 and FF_2. Dividing signals by two also divides their phase difference, extending range of circuit (A) from 180° to 360°. Four-gate exclusive-OR phase comparator modulates pulses, which then are filtered for analog output (B) to deflect meter.



(A) DIGITAL PHASE METER

(B) MEASURED PHASE DIFFERENCE

Counting by halves simplifies odd-order symmetric counter

by Edward J. Murray
Philco-Ford Corp., Willow Grove, Pa.

Odd-order countdown chains (such as divide-by-three and divide-by-five schemes) frequently involve intricate designs because there are no readily available devices. Using logic propagation delay and feedback to produce half-counts solves the problem. If the output of an n+1 counter (where n is odd) is fed back to either the input clock or its inverse, the counter can move half a clock phase during each transition of its output flip-flop. The resultant circuit output is an (n+1)−1=n count that is symmetric.

For example, a symmetric divide-by-three counter (A) can be realized with two flip-flops connected as a simple divide-by-four counter. Both outputs of the last flip-flop are fed back to select the appropriate clock phase. The configuration actually consists of a divide-by-1.5 stage followed by a divide-by-two stage, thus producing a symmetric divide-by-three counter.

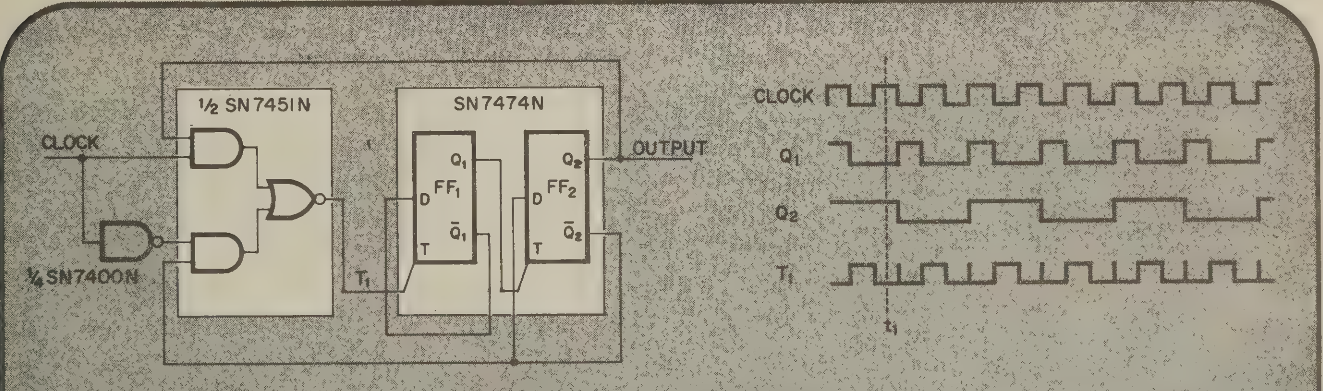
The Q_1 output of FF_1 provides the unsymmetric divide-by-1.5 count, which is used to toggle FF_2. The Q_2 output of FF_2 supplies both the symmetric divide-by-three count and the gating needed to determine what clock phase will be used. When FF_2 changes state, clock phase also changes.

The very narrow (less than 100-nanosecond) pulses present in the trigger signal T_1 are due to logic propagation delay. The first positive clock transition after time t_1 causes Q_1 to go high and Q_2 to go low so that the input clock toggles FF_1 directly. Each transition of FF_2 produces a phase change at the toggle of FF_1, causing spikes due to signal delay through the flip-flops.

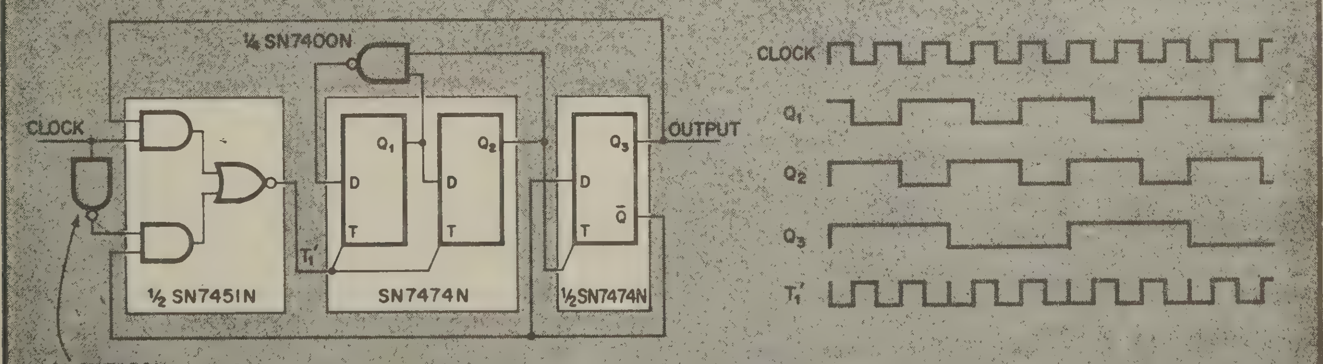
A symmetric divide-by-five counter (B) from a divide-by-six configuration operates similarly. Further extensions of the basic circuit principle also are possible. The logic modules used are made by Texas Instruments.

Applications for an odd symmetric counter include deriving a square wave from a master clock, full-duplex modems, multiplexers, special-purpose processors, multifrequency wave generators, and center-sampling systems. In general, these counters can be used whenever a square wave is needed for time-sharing equipment or for split-phase operations that must be synchronized to a variable master clock.

Countdown. Transitions of last flip-flop change phase (by half counts) of input clock, which controls toggle of previous flip-flop(s). Output of odd-order countdown scheme is symmetric square wave because final stage "divides evenly." Divide-by-three counter (A) can be extended into divide-by-five configuration (B) by adding another flip-flop and appropriate toggle controls.



(A) DIVIDE-BY-THREE COUNTER



(B) DIVIDE-BY-FIVE COUNTER

Seven-code PCM converter clocks at data output rate

by Jan Jansen
Data-Control Systems, Inc., Danbury, Conn.

A seven-code pulse-code-modulation converter can easily be made to perform at a data rate limited only by the capability of the logic used. The key element is a network that delays the clock so that the latter's frequency is the same as the output data rate. Conventional PCM converters usually employ a clock frequency of twice the output bit rate—for example, a data rate of 10 megabits per second normally requires a 20-megahertz clock. The code converter of (A), however, provides this output speed with only a 10-MHz clock.

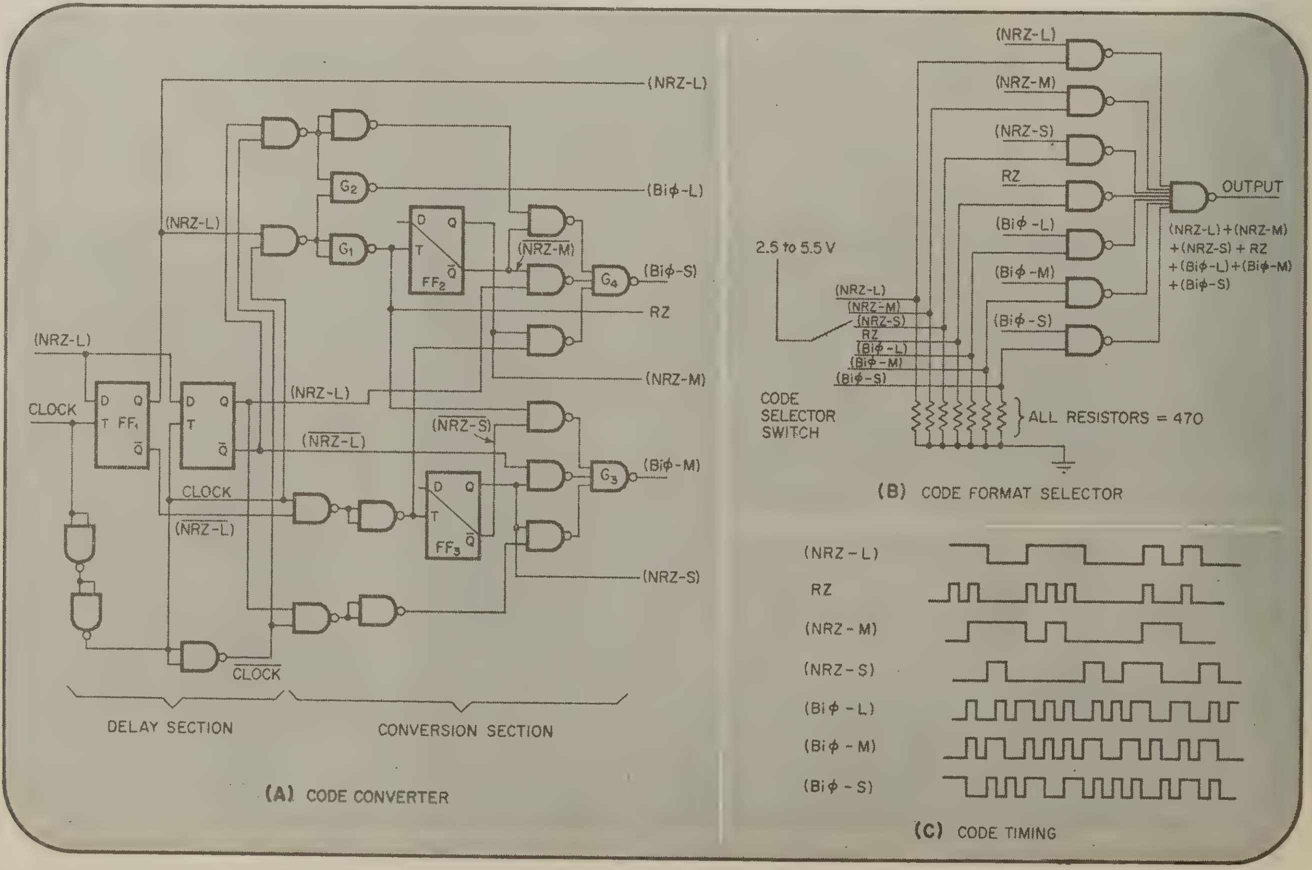
The "double clock" in conventional converters solves a problem called racing. If clock frequency is too low, small spikes, several nanoseconds wide, occur when the trailing edge of a coded signal coincides with the leading edge of a clock signal, or vice-versa. However, racing can be eliminated by delaying the transition of both signals. The clock starts to rise (or fall) only after the coded signal completes its level change from high to low (or low to high).

Because of the direct logic relationships between standard PCM codes, a relatively uncomplicated network of NAND dates and flip-flops enables the code converter to produce seven different codes simultaneously with only an NRZ-L (non-return-to-zero-level code) input. These are: NRZ-L itself, NRZ-M (non-return-to-zero-mark code), NRZ-S (non-return-to-zero-space code), RZ (return-to-zero code), Biϕ-L (biphase-level code), Biϕ-M (biphase-mark code), and Biϕ-S (biphase-space code).

The code converter consists of two basic sections. The first delays the data input, the clock and their complements; the second performs the actual conversions. Delay time is simply a function of signal propagation through the logic circuits.

The NRZ-L output only requires the delay provided

Delay pays. PCM converter (A) uses propagation delay of its logic elements to eliminate spikes during signal level transitions. This allows the circuit to work at a data bit rate equal to its clock frequency. Conversion speed is limited only by the logic used. Logic manipulation of input code results in six other PCM data outputs. Switching network (B) permits code selection. Code timing (C) is also shown.



by FF_1 and a normal (undelayed) clock:

(NRZ-L) = delayed (NRZ-L)

The other outputs require a delayed version of both the input code and the clock. The RZ output from G_1 is:

RZ = (NRZ-L) (clock)

The NRZ-M output from FF_2 becomes:

$$
\begin{aligned}
(\mathrm{NRZ}-\mathrm{M})_{tn} = {} & [(\mathrm{NRZ}-\mathrm{L})\,\overline{(\mathrm{NRZ}-\mathrm{M})_{tn-1}}] \\
& + [\overline{(\mathrm{NRZ}-\mathrm{L})}\,(\mathrm{NRZ}-\mathrm{M})_{tn-1}]
\end{aligned}
$$

where t_n represents the nth bit time.

The NRZ-S output from FF_3 is:

$$
\begin{aligned}
(\mathrm{NRZ}-\mathrm{S})_{tn} = {} & [(\mathrm{NRZ}-\mathrm{L})\,(\mathrm{NRZ}-\mathrm{S})_{tn-1}] \\
& + [\overline{(\mathrm{NRZ}-\mathrm{L})}\,\overline{(\mathrm{NRZ}-\mathrm{S})_{tn-1}}]
\end{aligned}
$$

The biphase codes are derived from the three non-return-to-zero codes. G_2's output yields:

$$
\begin{aligned}
(\mathrm{Bi}\,\phi-\mathrm{L}) = {} & [(\mathrm{NRZ}-\mathrm{L})\,(\mathrm{clock})] \\
& + [\overline{(\mathrm{NRZ}-\mathrm{L})}\,\overline{(\mathrm{clock})}]
\end{aligned}
$$

G_3's output is:

$$
\begin{aligned}
(\mathrm{Bi}\,\phi-\mathrm{M}) = {} & [(\mathrm{NRZ}-\mathrm{S})\,\overline{(\mathrm{NRZ}-\mathrm{L})}] \\
& + [(\mathrm{NRZ}-\mathrm{S})\,(\mathrm{NRZ}-\mathrm{L})\,\overline{(\mathrm{clock})}] \\
& + [\overline{(\mathrm{NRZ}-\mathrm{S})}\,(\mathrm{NRZ}-\mathrm{L})\,(\mathrm{clock})]
\end{aligned}
$$

G_4 provides the last biphase code:

$$
\begin{aligned}
(\mathrm{Bi}\,\phi-\mathrm{S}) = {} & [(\mathrm{NRZ}-\mathrm{M})\,\overline{(\mathrm{NRZ}-\mathrm{L})}\,(\mathrm{clock})] \\
& + [\overline{(\mathrm{NRZ}-\mathrm{M})}\,(\mathrm{NRZ}-\mathrm{L})] \\
& + [\overline{(\mathrm{NRZ}-\mathrm{M})}\,\overline{(\mathrm{NRZ}-\mathrm{L})}\,\overline{(\mathrm{clock})}]
\end{aligned}
$$

A suggested code format selector is shown in (B). All logic circuits are series 54/74 TTL ICs.

Short-delay J-FET switch gates high-speed data

by Edward S. Donn
Hewlett-Packard Co., Colorado Springs, Colo.

The distribution of high-speed digital data usually is slow compared to the logic handling the data. In measurement applications, for example, a command from a front-panel switch frequently is used to change the operating mode of an instrument by rerouting an internal signal. In a computer, a high-speed register may be switched (again, from the front panel) from one arithmetic unit to another. Very fast logic gates can distribute the data, but they are costly and waste logic power.

A junction field effect transistor circuit will do the job for a little more than $1—and with a propagation delay of less than 1 nanosecond. Although a FET switches slowly, it is an effective control element because its low on resistance allows it to pass digital data with very little delay. Moreover, signal reproduction is excellent.

The J-FET in the circuit is on when its gate-to-source voltage is zero, and off when this voltage is negative. Gate-to-source voltage is clamped to zero by R_1 and D_1.

The control signal is represented as a low-speed switch (B and $\bar{B}$). With a positive supply voltage applied to the J-FET and the control signal at location $\bar{B}$, the circuit performs an OR logic operations:

$C = A + \bar{B}$

If the control signal switches to location B, the J-FET turns on because its gate-source voltage becomes zero.

When a negative voltage is supplied to the J-FET and the control signal is at B, the circuit acts like an AND gate:

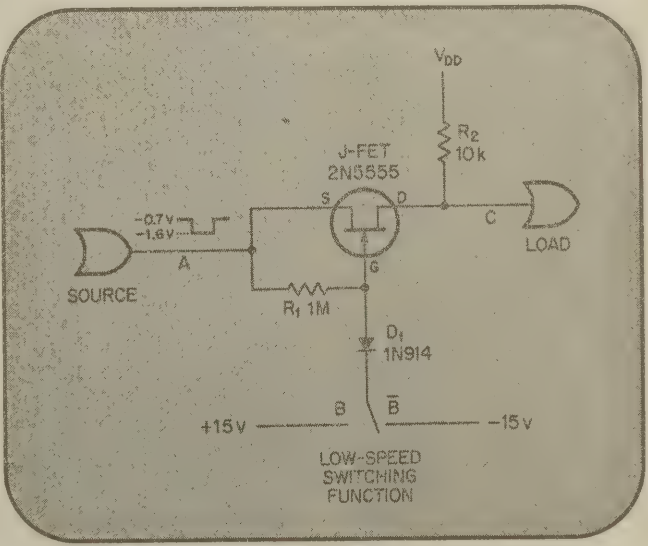
$C = A\,B$

The J-FET will turn off with the switch at $\bar{B}$.

Network propagation delay from A to C is determined by the J-FET's on resistance and the parasitic capacitance at C caused by the load and J-FET gate-drain capacitance. For a resistance of 150 ohms and a total capacitance of 5 picofarads, the delay is just 0.55 ns.

Resistor R_1 must be small enough to pass gate leakage current from the J-FET but large enough to avoid loading the source applied at A. Resistor R_2 biases the load connected at C. If the load is an emitter-coupled logic gate, R_2 can be made large (10 kilohms for the circuit shown).

Instead of a J-FET, an insulated-gate field effect transistor may be used, eliminating the need for R_1 and D_1. Even a FET inside a multiple-transistor IC package will perform the circuit function. However, these ICs are more expensive than discrete J-FETs and tend to increase propagation delay. The substrate capacitance of transistor arrays usually more than doubles the parasitic capacitance that must be driven by the source at A. If the size of the circuit can be accommodated, discrete J-FETs are the best choice.



Digital switch. Low on resistance of J-FET enables it to handle high-speed digital data. With positive supply, circuit is an OR gate ($C = A + \bar{B}$); with negative supply, an AND gate ($C = AB$).

Variable oscillator controls pulse width and spacing

by A. Cavit and S. Bracho
University of Seville, Spain

Independently varying the pulse and interpulse times of a voltage-controlled oscillator makes the circuit useful for analog computing, telecontrol, and telemetry applications. The oscillator can serve as an adder, a subtractor, a function generator, or a multiplexer. With modifications, it can be a multiplexer or an inverse function generator.

Basically, the circuit is a two-stage relaxation oscillator that controls output pulse duration with one signal, E_1, and the time between pulses with another signal, E_2. Each stage contains a Miller integrator, which operates as a sawtooth pulse generator, and a comparator.

Signals E_1 and E_2 can be detected individually after transmission or magnetic recording on a single channel. Three signals may be detected if the third amplitude-modulates the other two.

When interstage switch Q_1 saturates, C_1 discharges and sets integrator A_1 to zero. This cuts off Q_1 so that C_1 charges and A_1's output rises linearly. When A_1's ramp level coincides with signal E_1, comparator A_2 changes state. Circuit on-time, kE_1, is related to the reciprocal of the sawtooth slope—k is about 6.2×10^{-5} seconds per volt.

While A_2 is high, Q_2 is saturated and C_2 discharges by being virtually shorted across Q_2's collector and emitter. Therefore, A_3 cannot start its ramp until A_2 changes state and cuts off Q_2. Also, comparator A_4 remains low until A_3's ramp and E_2 coincide. Circuit off-time or interpulse period becomes kE_2.

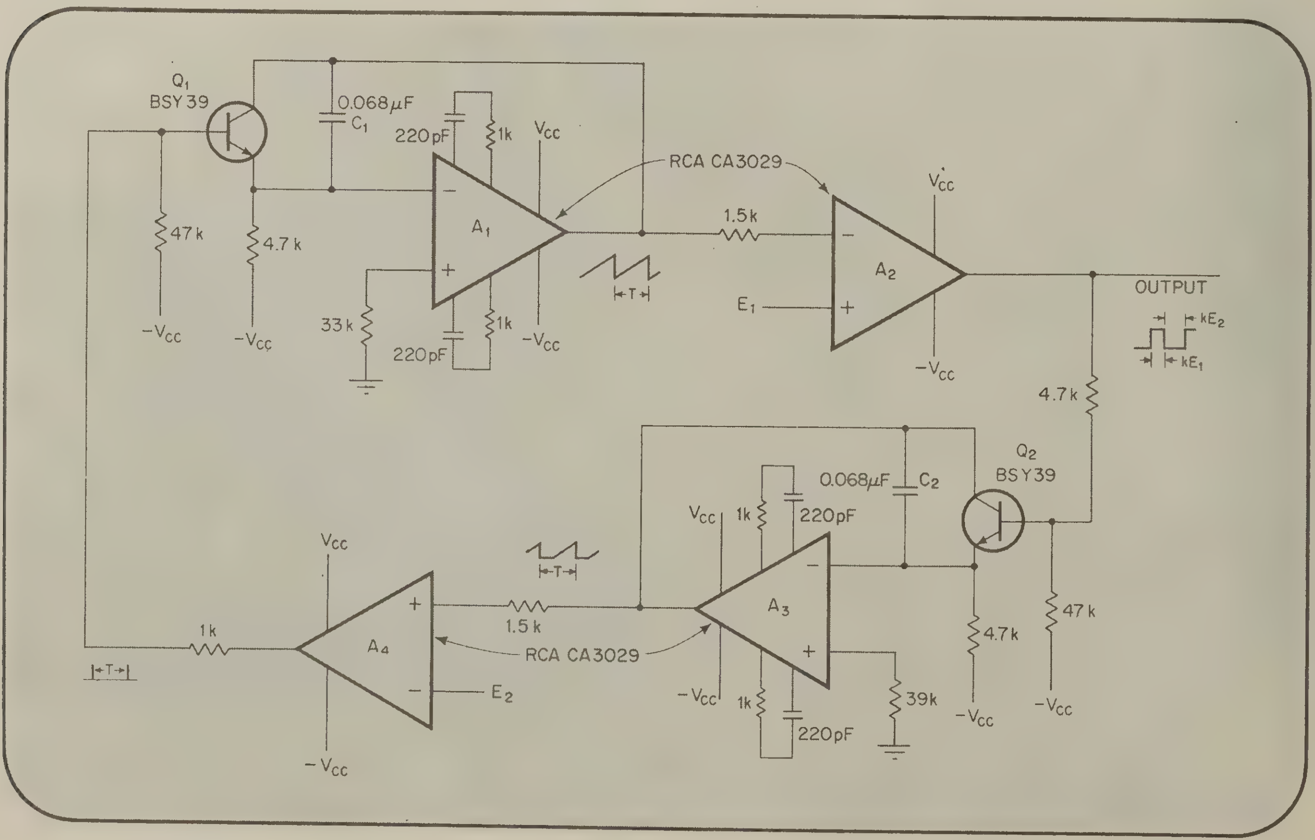
When A_4 changes state, its output is only a brief pulse (2 microseconds or less) occuring once in each oscillator period. Q_1 saturates for only a short time and discharges C_1. The circuit cycle can now repeat.

If $E_1 = E_2$, the output will be a square wave; if $E_2 = 2E_1$, the output period will be 50% longer. Moreover, it is possible to obtain E_2/E_1 by detecting the mean value of the output voltage when E_1 modulates pulse width and $(E_2 - E_1)$ modulates interpulse time.

Circuit operating frequency can range from 2 to 20 kilohertz. Pulse width is variable from 30 to 250 µs as E_1 goes from 0.5 to 4 V. Interpulse period is also adjustable—from 20 to 250 µs for E_2 variations of 0.3 to 4 V. However, control voltages of 0.5 to 2 V are recommended in order to stay within the operating limits of the type CA3029 amplifier. Comparator precision is ±3 millivolts.

The diagram shows European transistors, type BSY39 (Miniwatt); the American type 2N3261 has similar performance characteristics. Supply voltages should be $V_{CC} = 9$ V and $-V_{CC} = -6$ V; but $V_{CC} = 6$ V can also be used with some reduction in operating frequency.

Computing oscillator. When the sawtooth generated by A_1 coincides with E_1, comparator A_2 changes state. Its output is a pulse whose width is proportional to E_1. Then A_3 and A_4 take over, resetting A_1 when A_3's sawtooth coincides with E_2. This makes the interpulse time, due to the output of comparator A_4, proportional to E_2. Frequency range for this VCO is 2 to 20 kilohertz.



Amplifier slew-rate curves simplify design decisions

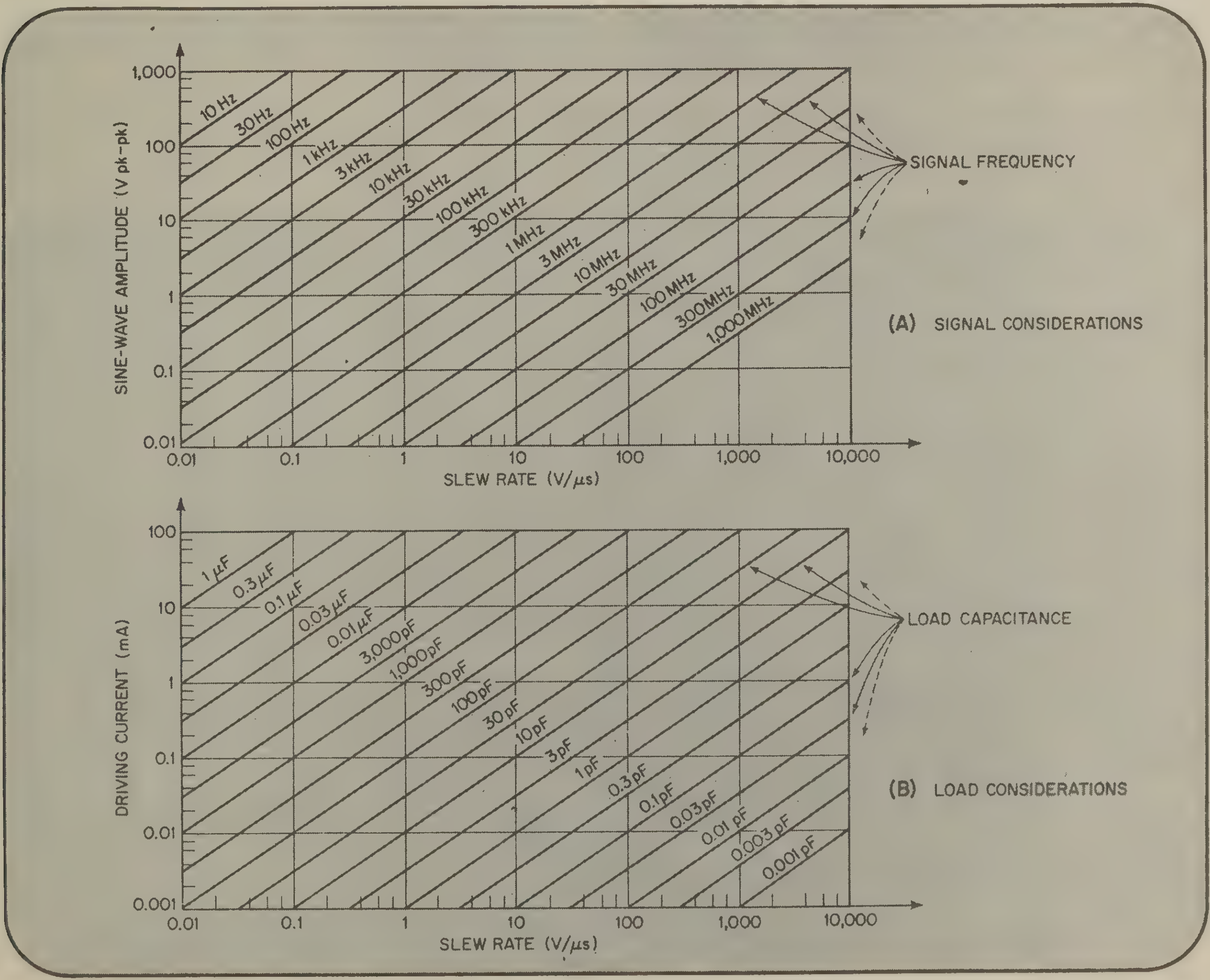
by H.A. Wittlinger
RCA/Electronic Components, Harrison, N.J.

Don't guess at the slew rate of an operational or broadband amplifier—instead, use the handy curves shown. They're important, because above dc, slew rate is directly proportional to the product of the output signal frequency and its peak-to-peak amplitude.

Illustration (A) makes it easy to find the slew rate an amplifier must have to produce a signal with a given voltage swing and frequency. It is derived from the maximum rate of change of a sine wave as it goes through its zero-crossing. The graph shows that a 1-megahertz sine wave, having a 1-volt pk-pk level, requires a slew rate of only 3.14 volts/microsecond, while a 5-V pk-pk signal at 5 MHz needs 78.5 V/μs.

Amplifier slew rate also is affected by available output load current and the load capacitance that must be driven. Illustration (B) is a plot of driving current as a function of slew rate with load capacitance as the third parameter. It is based on the equation, $dV/dt = I/C$, where dV/dt is the slew rate (V/μs), I the driving current (amperes), and C the load capacitance (microfarads).

An amplifier must provide sufficient driving current for a given capacitive load and pk-pk signal swing at a specified operating frequency. For a slew rate of 3.14 V/μs (for 1-MHz, 1-V pk-pk signal), output current must be 0.94 milliampere to drive a 300-picofarad load, and 9.4 mA for a 3,000-pF load. When slewing increases to 78.5 V/μs (for 5-MHz, 5-V pk-pk signal), current demand rises to about 23.5 mA for the 300-pF load and to more than 100 mA (to 235 mA, which is beyond the graph) for the 3,000-pF load. Obviously, in order to supply a high slew rate, an amplifier must be able to deliver a high output current at the same time.



Design aids. Use a ruler and graph (A) to determine op-amp slew rate needed for specific output signal frequency and voltage swing. Then apply the ruler to graph (B) and find current needed to drive given load capacitance. Curves help establish minimum operational amplifier requirements for designing ac circuits.

Gated clock cuts counter delay to 60 ns

by Edward E. Pearson
Dunedin, Fla.

If cascaded decade counters operate from a gated clock, their propagation delay is independent of the number of counter stages, even when their outputs must be read as the count continues. Propagation delay remains at only 60 nanoseconds, yet counting rates can be more than 10 megahertz. In such a counter (A), the stages are linked by TTL AND gates and employ a common clock bus like the one used in a synchronous counter.

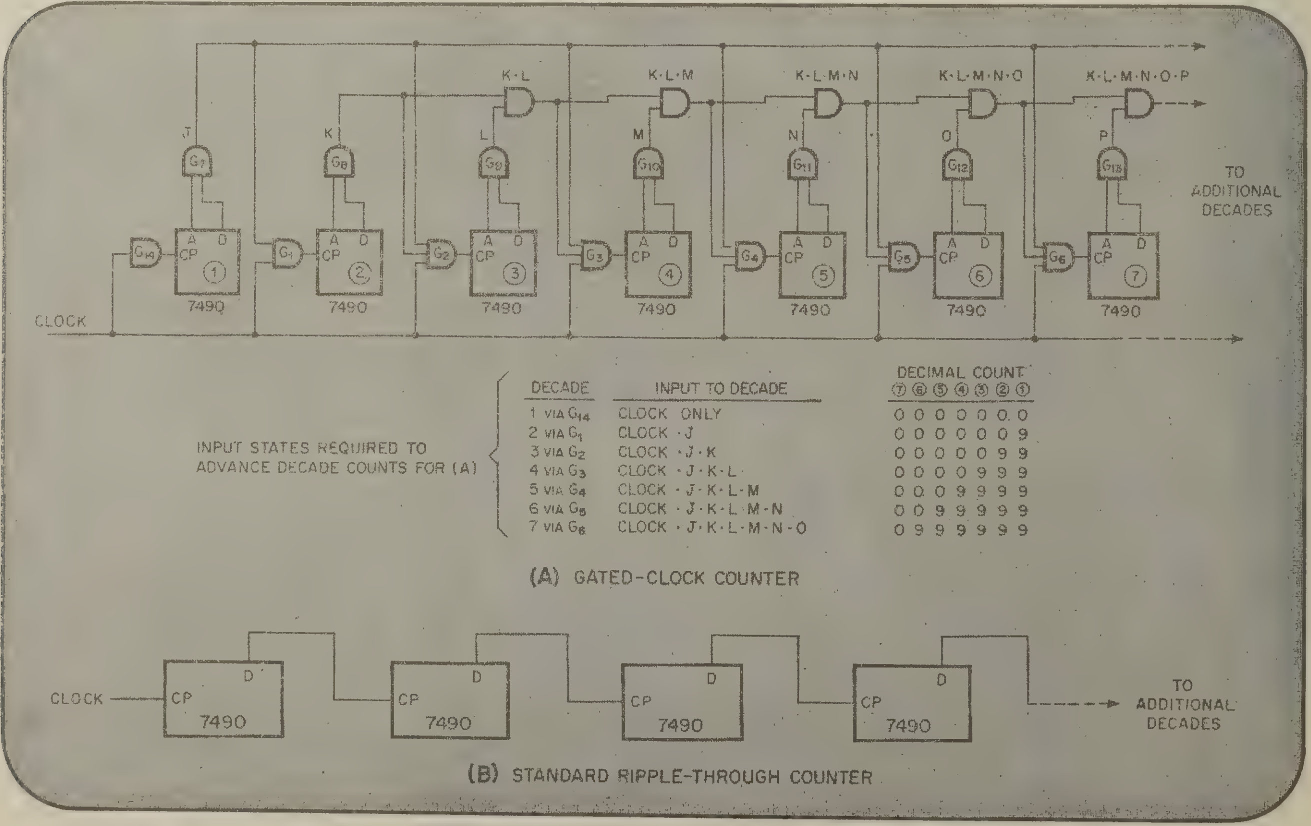
A conventional ripple-through arrangement (B) usually involves a propagation delay as large as 60 ns for each decade when synchronous parallel readout is required. As a given decade's D output goes from high to low, it toggles the input of the following decade. These transitions must ripple down the entire chain of decades so that the last decade can reach the proper count for a true parallel readout to be available. A transition from 0999999 to 1000000, for example, normally requires about 400 ns, and limits clock rate to around 2 MHz.

Any given decade in the improved counter receives its clock pulse only after all the decades preceding it have reached the count of nine (both the A and D outputs are high). To control the gating of the clock pulses, the A and D outputs of each stage go through a sequence of AND gates from one decade to the next.

The clock input gates, G_1 through G_6, are conditioned before the arrival of the next clock pulse because gates G_7 through G_{13} go high on the trailing edge of positive pulses. In one clock period, the first (least-significant) decade counts from 0 to 9. Therefore, G_7 stays high for only one clock period, G_8 for 10 periods, G_9 for 100, G_{10} for 1,000, and so on. The longest propagation path runs from G_8 to the most distant decade input gate (G_6 for the configuration shown).

This gated clock scheme can also be used to reduce system delay for a chain of synchronous decade counters, such as the 74192, by eliminating cumulative overflow gate delays.

Sharing the clock. Decade in gated-clock scheme (A) receives clock pulse only if less-significant decades before it have each counted to 9. The input clock gate for each stage operates from a common clock bus. Although one clock operates all decades, propagation delay is not affected by the number of stages. Conventional scheme (B) requires clock to ripple-through until last decade has reached the proper count.



INPUT STATES REQUIRED TO ADVANCE DECADE COUNTS FOR (A)

DECADE	INPUT TO DECADE	DECIMAL COUNT ⑦ ⑥ ⑤ ④ ③ ② ①
1 VIA G_{14}	CLOCK ONLY	0 0 0 0 0 0 0
2 VIA G_1	CLOCK · J	0 0 0 0 0 0 9
3 VIA G_2	CLOCK · J · K	0 0 0 0 0 9 9
4 VIA G_3	CLOCK · J · K · L	0 0 0 0 9 9 9
5 VIA G_4	CLOCK · J · K · L · M	0 0 0 9 9 9 9
6 VIA G_5	CLOCK · J · K · L · M · N	0 0 9 9 9 9 9
7 VIA G_6	CLOCK · J · K · L · M · N · O	0 9 9 9 9 9 9

(A) GATED-CLOCK COUNTER

(B) STANDARD RIPPLE-THROUGH COUNTER

Shorted load folds back supply current

by Benjamin Stopka
Fairport, N.Y.

Having a foldback current-limiting capability in power supplies can save much grief during circuit breadboarding and debugging. The protection against shorts costs less than $1 in extra voltage-regulator parts—well worth it if, for example, an overload doesn't burn out an expensive transistor.

Voltage regulators typically deliver more current after a short than before (curve A). Sharp foldback (B) shuts off the supply almost instantly. A compromise (C) keeps the supply working into high-capacitance loads and avoids the bother of unlatching it. Foldback is adjustable.

Transistor Q_1 and resistor R_1 are the standard protective parts. At point 1 on the curves, Q_1 becomes forward-biased and diverts some base current away from pass transistor Q_2. The regulator then becomes a constant-current source; V_{out} drops as R_{load} approaches zero ohms.

However, as Q_2 is losing base current and becoming more resistive, the current into the load is not merely the overload value at point 1 (about 370 milliamperes if IR/R_1 is approximately 0.55 volt/1.5), but includes current from Q_2, base resistor R_2 and A_1. The error-amplifier output rises as V_{ref} exceeds V_{out}. The additional currents readily exceed tens of milliamperes.

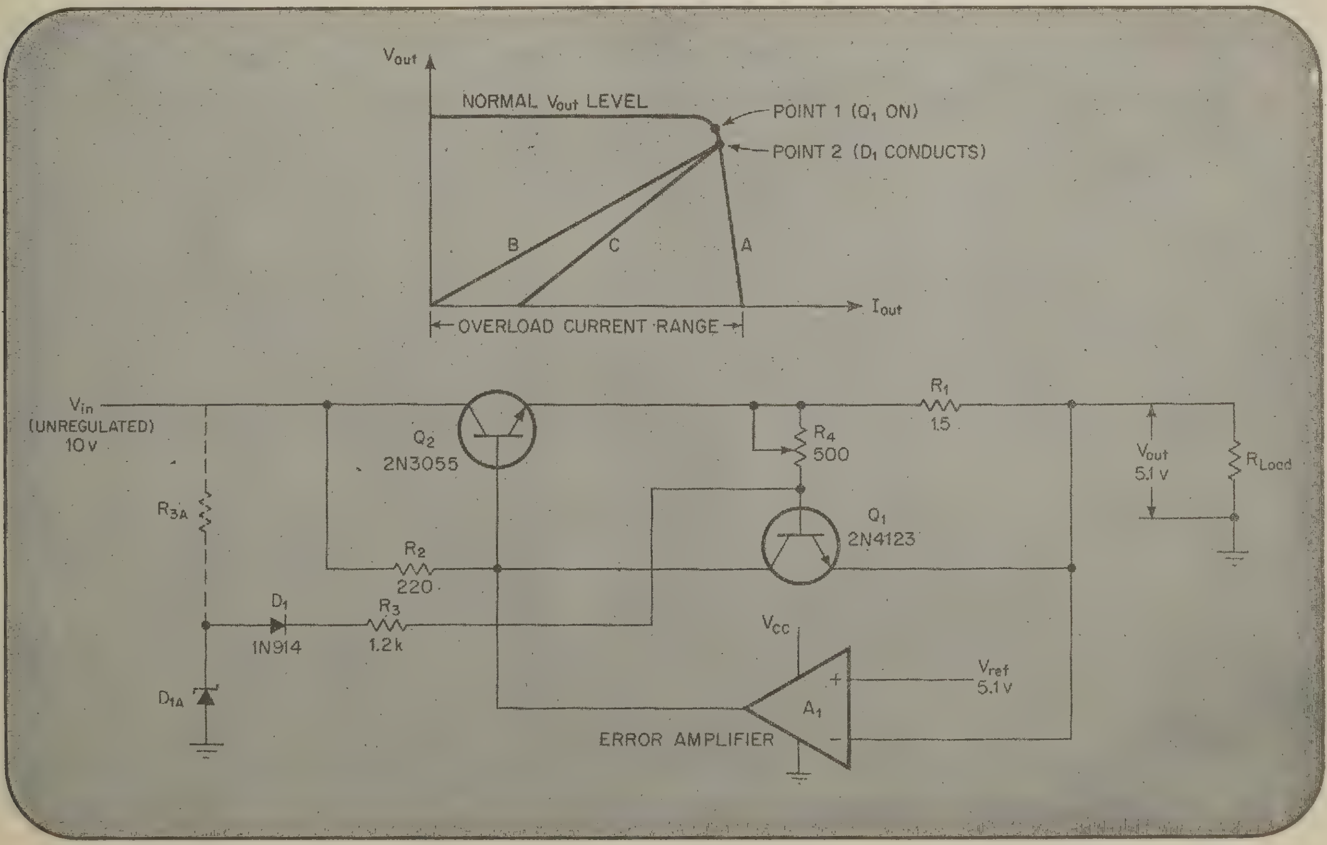
With diode D_1 and R_3 in the circuit (and potentiometer R_4 set to zero ohms), Q_1 operates as before. D_1 becomes forward-biased at point 2, and V_{ref} supplies current through R_3 to help forward-bias Q_1. Because R_3's current is small compared to the regulator current supplied by Q_2, the I-V slope will maintain its similarity to curve A, which crosses the I_{out} axis at about 430 mA.

If R_4 is set to maximum, curve B results. At point 2, V_{ref} supplies current to Q_1's base and R_4, resulting in an increase in Q_1's forward-biasing. More importantly, as V_{out} drops, Q_1 turns on more fully and Q_2 turns off, eliminating most of the current through R_1. Essentially, the regulator will supply only the current diverted through Q_1 from R_2 and A_1, which drops the overload current sharply.

However, the regulator cannot restart unless the value of R_4 is reduced. The smaller current through R_4 and its attendant voltage drop tends to keep Q_1 on, which reverse-biases Q_2. With the regulator output shorted, R_4 can be adjusted so that the I-V curve will intersect the I_{out} axis at a location that prevents latchup.

D_1 and R_3 should be connected to D_{1A} and R_{3A} if V_{out} is much larger than V_{ref}. The alternate overload reference voltage should correspond to point 2 so that D_1 becomes forward-biased at approximately the same V_{out} level as before.

Underload supply. Components shown in color will prevent the voltage regulator from raising the overload current when the load shorts. The current can be folded back between curves A and B to any slope C by adjusting R_4. At point 1, Q_1 starts diverting Q_2's base current. Diode D_1 conducts at point 2, minimizing current generation in R_1 and Q_2. Components D_{1A} and R_{3A} must only be used if V_{out} is much larger than V_{ref}.



Versatile digital circuit filters highs, lows, or bands

by Ronnie Jack McKinley
Halliburton Research Center, Duncan, Okla.

A digital filter doesn't have to be complex to provide low-pass, high-pass, bandpass or band-reject functions. All it takes is a simple combination of gates, flip-flops, and inverters. Because it's digital, the circuit yields an almost ideal filter response for a square wave.

The break frequency, f_o, for the low-pass or high-pass digital filter (A) is determined by R_1 and C_1. These two components therefore also set the one-shot's gate time, τ, which is half the period (T_o) of the break frequency.

$f_o = 1/T_o = ½\tau = ½R_1C_1$

where $\tau = T_o/2 = R_1C_1$

The first positive-going edge of the input square wave turns on the one-shot for its preset gate time. AND gate G_1 is enabled by the one-shot, while AND gate G_2 is inhibited.

If the square-wave frequency is higher than f_o, gate G_1 produces an output pulse that latches flip-flops FF_1 and FF_2. The output from FF_1 enables AND gate G_3, which lets the input signal pass through to the circuit output. Gate G_2 remains inhibited during this time.

When the input frequency falls below f_o, gate G_1 is inhibited while G_2 becomes enabled and resets FF_1. This inhibits G_3 and stops the incoming square wave from propagating to the output.

Flip-flop FF_2 prevents false triggering of FF_1 at high frequencies. It is reset at the start of each one-shot gate.

A simple circuit modification converts the high-pass digital filter to a low-pass function. All that's required is placement of an inverter between the output of FF_1 and the input of G_3. Break frequency remains the same.

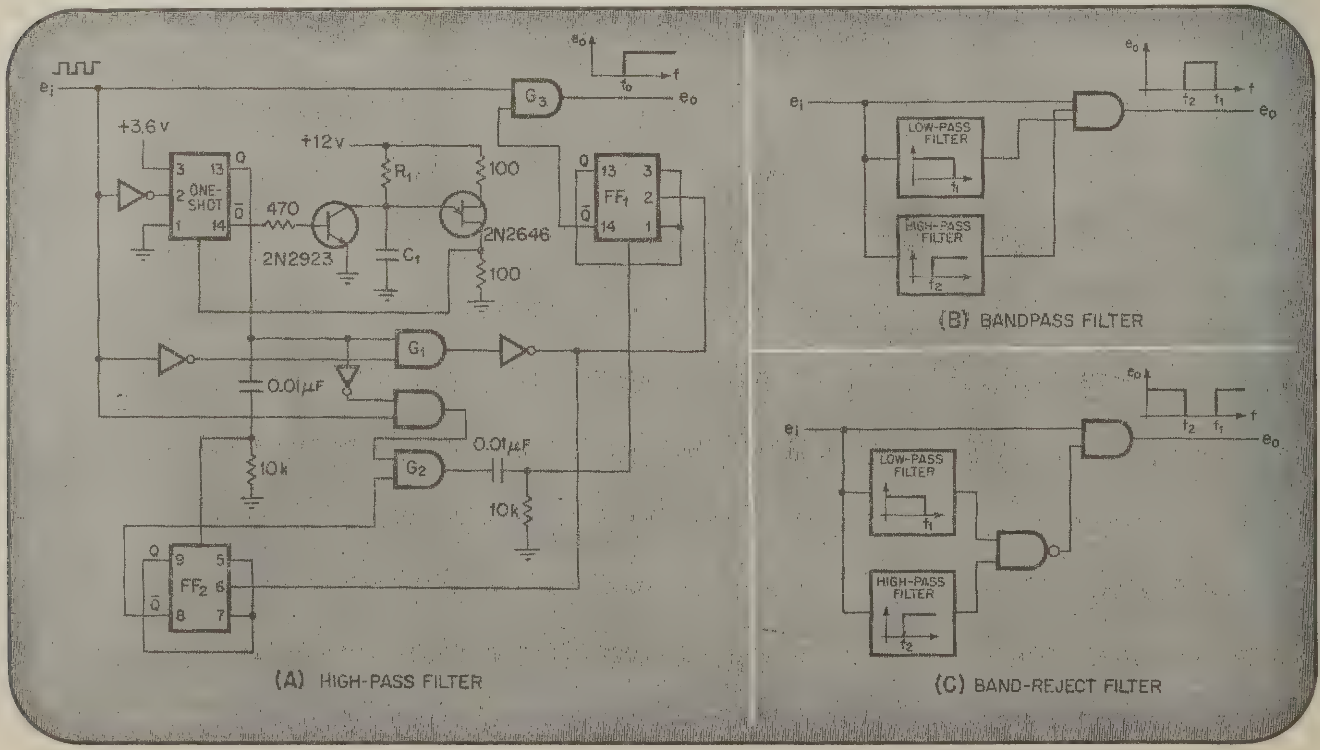
A bandpass digital filter (B) can be made by feeding the input signal and the outputs of a low-pass filter and a high-pass filter into a triple-input AND gate. For the bandpass function, the break frequency of the low-pass circuit, f_1, must be higher than the break frequency of the high-pass circuit, f_2.

Similarly, the band-reject response (C) can be realized with two filter networks controlled by a dual-input NAND gate and a dual-input AND gate at the output. Again, the low-pass break frequency (f_1) must be greater than the high-pass break frequency (f_2).

These digital filters can function with any periodic input signal if it is first squared to obtain sufficient amplitude for operating the logic circuitry. The frequency range for each filter type is limited only by the duty cycle of the one-shot and the speed of the logic.

The one-shot (Motorola MC790P) in the basic filter is a high-duty-cycle monostable that remains on for a constant period of time once it is triggered. The other circuit components are Motorola MC9713P dual-input gates, Motorola MC790 P R-S flip-flops, and a Motorola MC789P hex inverter. Resistor R_1 and capacitor C_1 can assume a broad range of values, depending on the speed of the logic and the quality of the capacitor.

Filtering digitally. High-pass digital filter (A) lets through frequencies above f_o when G_1 latches FF_1 so that G_3 is enabled. G_2 resets FF_1, inhibiting G_3 if the input is less than f_o. One-shot gate time determines f_0. A high-pass circuit can be converted to a low-pass one by inverting FF_1's output to G_3. Bandpass (B) and band-reject (C) functions are implemented by controlling two basic filters with gates.

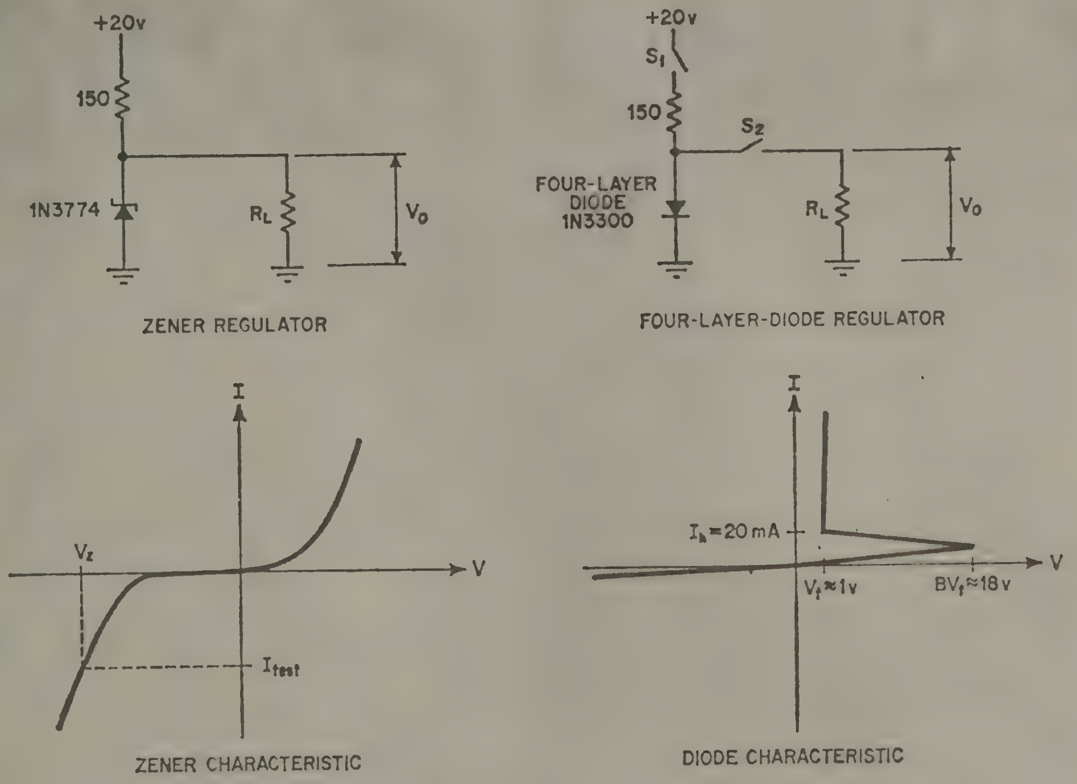


Four-layer diode circuit out-regulates zener by 5:1

by R.D. Clement and R.L. Starliper
Western Electric Co., Burlington, N.C.

A four-layer diode can provide five times better regulation than a zener diode when load voltage is less than 6.2 volts. The diode configuration can operate with the same supply voltage as the zener circuit and can drive an identical load resistance. However, voltage regulation from a no-load to full-load condition is approximately 6% for a diode regulator with an output voltage of 1V, while it approaches 30%

Diode versus diode. Avalanche current of four-layer-diode's on characteristic maintains almost constant output voltage despite increased current demand from low-resistance load. Zener circuit loses regulation with decreasing load because device current drops, pulling output voltage down with it.



ZENER REGULATOR

FOUR-LAYER-DIODE REGULATOR

ZENER CHARACTERISTIC

DIODE CHARACTERISTIC

REGULATOR COMPARISON

ZENER DIODE		FOUR-LAYER DIODE	
R_L (OHMS)	V_o (VOLTS)	R_L (OHMS)	V_o (VOLTS)
∞	1.56	∞	1.02
470	1.55	470	1.02
100	1.53	100	1.00
30	1.46	30	0.98
15	1.34	15	0.97
10	1.13	10	0.96

for a zener circuit.

Most zener diodes provide poor regulation below 6.2 V because they do not operate with a true avalanche effect. To obtain the desired output voltage (V_z), the zener must be operated at the test current (I_{test}) specified by the manufacturer. Since the load resistance requires more current as it goes from a high value to a low one, current through the zener decreases and its output voltage drops. The result is poor voltage regulation.

Because of the nature of its on characteristic, a four-layer diode overcomes this problem. With both switches open, the diode circuit is not energized. When S_1 is closed, the voltage across the diode increases until it reaches the device's forward breakdown voltage ($BV_f \approx 18$ V). Then the diode conducts because avalanche breakdown occurs, and diode voltage drops to 1 V.

Now S_2 can be closed, applying voltage to the load resistance, R_L. To maintain regulation, the current through the diode must be greater than its hold current ($I_h = 20$ milliamperes for the 1N3300). Diode voltage ($V_f \approx 1$ V) is not degraded with decreasing load resistance because the device exhibits a nearly ideal avalanche effect.

Regulated voltage can easily be increased—for example, to 3 V—by connecting several four-layer diodes in series and increasing the supply voltage accordingly. The approximate parts cost for the diode regulator is $5.90, and $3.25 for the zener circuit. S_1 and S_2 are single-pole single-throw switches like the Alcoswitch MSP103C.

Diodes stabilize FET gain to 1% over 100°C range

by Donald F. DeKold
Santa Fe Junior College, Gainesville, Fla.

Gain variations in a field effect transistor can be reduced to less than 1% over a 100°C temperature range by putting conventional diodes and negative feedback in the FET's gate-source loop. Without this compensation, gain is higher, but decrements in gain can reach 30% as temperature rises to 100°C.

The small-signal voltage gain of an uncompensated, single-stage FET amplifier frequently deteriorates drastically with increasing temperature. For example, circuit (A) has a gain of 30 at 0°C, decreasing to only 21 at 100°C. This reduction occurs primarily because the FET's transconductance (g_m) is temperature-sensitive. Bias conditions, like drain current (I_D), gate-source voltage (V_{GS}), and drain-source voltage (V_{DS}) change little due to the high degree of existing dc feedback.

Inserting a few standard diodes in the FET's gate-source loop (B) stabilizes amplifier gain without adding more stages. As temperature increases, the forward-voltage drop of each diode decreases, thus reducing V_{GS}.

If temperature were constant, a drop in V_{GS} would raise the FET's transconductance as its bias point moves. But since temperature is changing, g_m remains constant while the bias point shifts from location 1 to 2 as indicated by the characteristic curve of (D). The change in bias conditions also lowers V_{DS} and raises I_D.

However, diode voltage change is not a sole function of temperature. Rather, a rise in drain-source current tends to increase diode forward drop, while rising temperature tries to reduce it. The net voltage change, according to measured data, moves the bias point so that g_m remains relatively constant within certain temperature intervals. For example, circuit (B) exhibits a virtually constant gain of 27 from 0 to 40°C; it drops by 6% at 100°C.

Introducing negative feedback in the gate-source loop reduces gain but provides stability. The amplifier of (C) gives a nearly constant gain of 11 from —10 to +50°C. Gain degrades by only 3% at a low of —30°C or at a high of 100°C. Careful selection of the bias point for this circuit and precise determination of the number of diodes can keep gain variations below 1% over a 100°C temperature interval.

The FET in these circuits has a pinch-off voltage (V_P) of —3.3 V and is biased at a V_{GS} of —3 V for 20°C. If a FET with a lower V_P is used, fewer diodes may be needed.

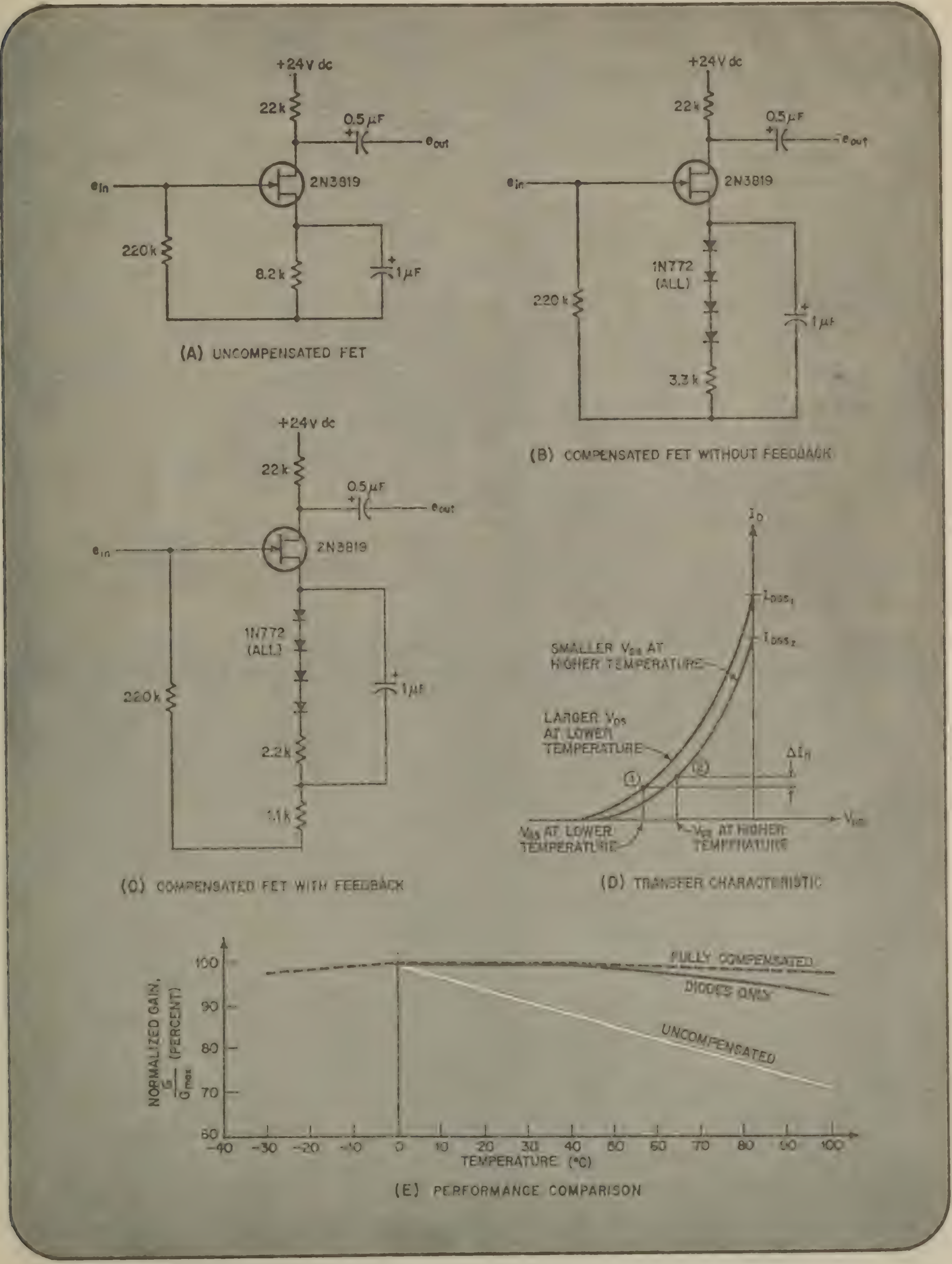
Also, V_{DS} should be several times larger than the voltage across the amplifier's load resistance. Load voltage almost doubles because of the increase in I_D and tends to decrease V_{DS}. Changes in V_{DS} should be kept relatively small, or the ratio of $\Delta V_{DS}/V_{DS}$ should be a low value.

The curves in (E) show the gain of each amplifier configuration normalized with respect to their maximum gains, which occur at a temperature of 0°C. The uppermost curve represents the fully compensated amplifier, which has a gain of 11 at 0°C. The bottom curve is for the uncompensated amplifier, whose gain is 20 at 0°C.

As can be seen, the gain of the fully compensated amplifier degrades only 3% (its gain drops to 10.7) when the temperature increases to 100°C. The uncompensated amplifier, however, experiences a gain degradation of 28% (its gain decreases to 21) as the temperature rises to 100°C.

Only the fully compensated amplifier operates at temperatures below 0°C. Its gain changes by only 3% when the temperature drops to —30°C.

Hold that gain. Diodes in gate-source loop of FET minimize gain variations without additional stages. As temperature rises, V_{GS} drops and shifts amplifier bias point. But gain changes very little because FET's g_m stays practically the same. Adding negative feedback provides even greater gain stability.



(A) UNCOMPENSATED FET

(B) COMPENSATED FET WITHOUT FEEDBACK

(C) COMPENSATED FET WITH FEEDBACK

(D) TRANSFER CHARACTERISTIC

(E) PERFORMANCE COMPARISON

Dual gate plus transistor generates 12 functions

by Edward B. Beach
National Radio Institute, McGraw-Hill Inc., Washington, D.C.

Marry two old solid state components—a dual RTL (resistor-transistor logic) NOR gate and a pnp transistor—and you get a surprisingly large family of signal generators.

First, connect gates G_1 and G_2 as a set-reset flip-flop, and clamp capacitor C_1 near ground with Q_1 in the quiescent state—that's when input A is low, output B is high, and outputs C and D are low.

Then to start, one short pulse into A sets B low and C high, turning Q_1 off. Current through R_1 starts charging C_1 towards 3.6 volts. However, when Q_1's emitter becomes about 0.6 V more positive than its base, Q_1 turns on and C_1 discharges rapidly through Q_1 into the lower input G_2. This resets the flip-flop and returns the circuit to its quiescent state.

Looking at the circuit outputs: B is a pulse delay, C is a monostable multivibrator, and D is a ramp generator. Periodically retriggering G_1 makes the circuit a relaxation oscillator at D and a step-pulse generator with complementary outputs at between B and C. It will also generate square waves, since duty cycles between 10% and more than 95% of the trigger period may be selected with R_2 and C_1.

Next, if the R_2C_1 time constant exceeds the trigger period, the circuit becomes a frequency divider. The B output is not very useful, but adjusting R_2C_1 readily makes the pulse frequency at C a submultiple of the trigger frequency.

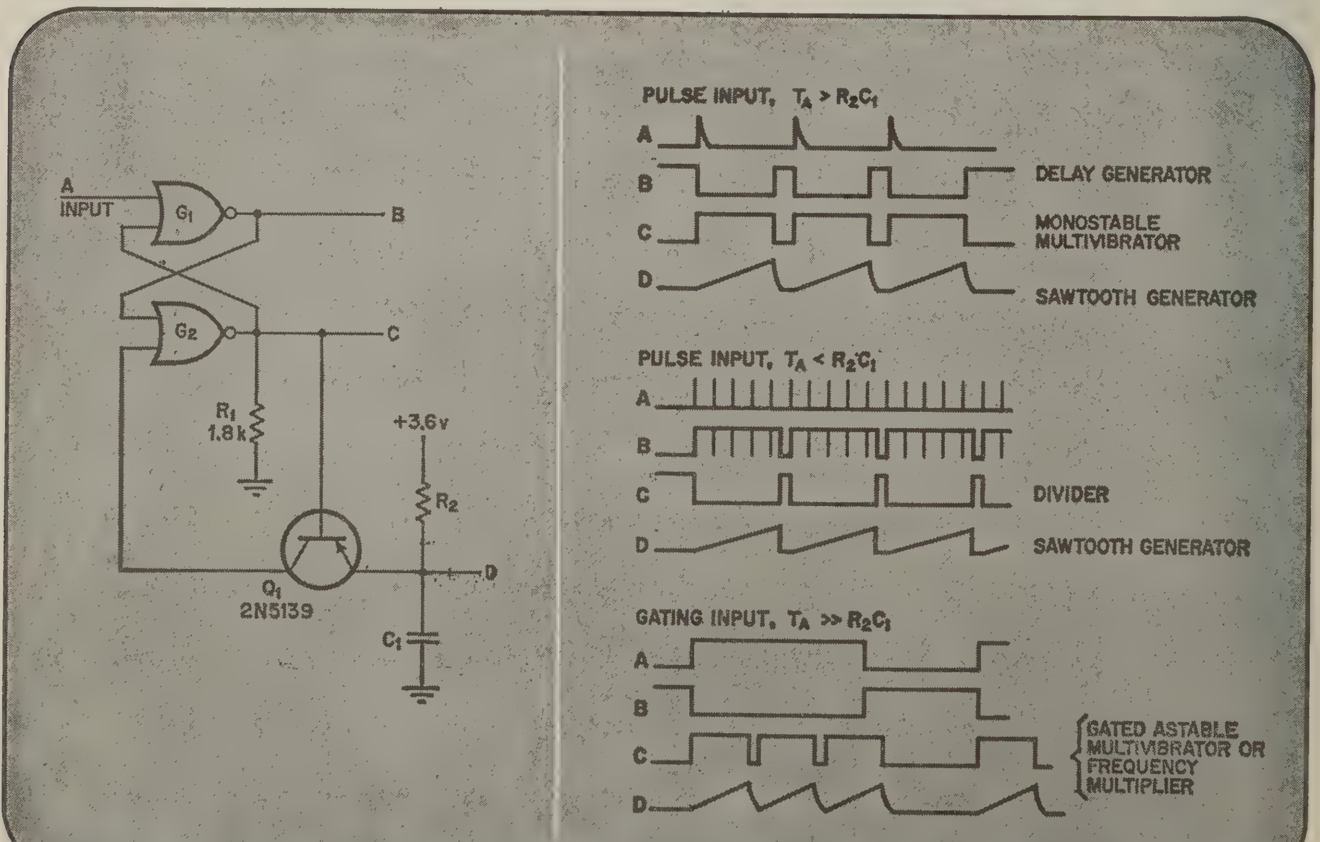
The circuit transforms itself into a gated astable multivibrator when the A input is held high. Alternatively, it acts as a frequency multiplier when the gating input is periodic. The C output is relatively independent of the A input, making adjustment easy.

Finally, R_2 may be replaced with a constant-current source. Now, the ramp at D becomes linear enough for other delay applications and for sweeping. Varying the input to the constant-current source gives a good pulse-width-modulated signal output at D.

Resistor R_2 can range from 4.7 to 220 kilohms, while C_1 can be 20 picofarads to 100 microfarads. This means that the R_2C_1 time constant can vary from 94 nanoseconds to 22 seconds.

The dual two-input gate can be a Fairchild μL914 or half a Motorola MC824P.

Select-a-pulse generator. Duration of the input pulses and their timing versus R_2C_1 determine the functions obtained at outputs B, C and D. While A sets the flip-flop, R_2C_1 determines the sawtooth generator period and the width of the pulses put out by the RTL gates. Every time the lower part of the circuit relaxes, the flip-flop is reset.



Flip-flop pair synchronizes pulses and floats clocks

by Lee E. Baker
University of Wisconsin, Madison, Wisc.

Two J-K flip-flops can do the work of a digital one-shot—and more. They can synchronize random events with clocks, change a square-wave signal generator into a pulse generator, and with a frequency divider modulate clock frequencies. Unlike a one-shot, pulse lengths and separations are widely and easily varied.

In the basic pulse separator's standby state, the two flip-flops are latched so the Q_1 output is low. When a reset pulse is applied, both flip-flops are unlatched. A trigger pulse to FF_1 causes Q_1 to go high (logic 1) and relatches FF_2. The action resembles a monostable multivibrator's, but the on time varies with the trigger period, the off time with the reset pulse period.

This action results from the J_1 and K_1 inputs to FF_1 changing state with FF_2 while the J_2 and K_2 inputs are grounded. During standby, $\overline{Q}_2$ and J_1 are 0 and Q_2 and K_1 are 1. Therefore Q_1 remains low regardless of the trigger pulses (a J-K flip-flop's Q output is forced to 0 by a trigger if J if 0 and K is 1).

A reset pulse on the R_2 input changes FF_2's state and resets J_1 and K_1. This allows FF_1 to change state on the next trigger-pulse trailing edge (the μL923 triggers on a trailing edge). Because J_1 is 1 and K_1 is 0, Q_1 goes high immediately. The drop of $\overline{Q}_1$ is seen by FF_2 as a trigger trailing edge, and FF_2 changes state, reverting to the standby condition.

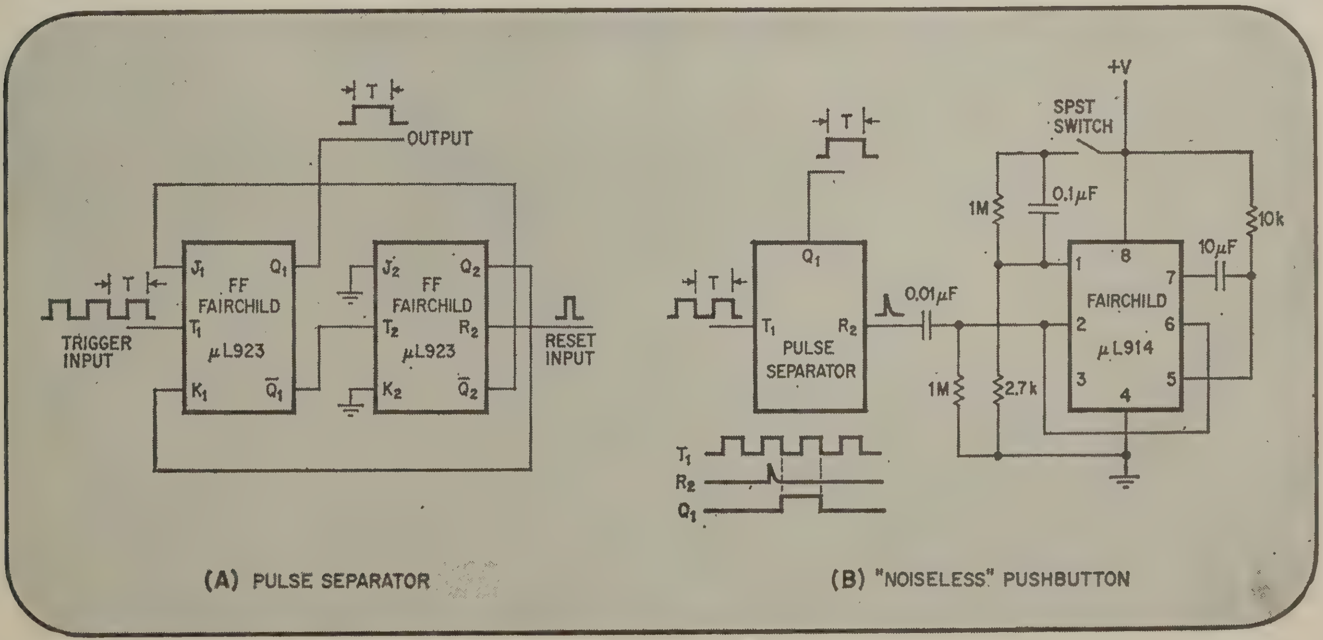
Consequently, Q_1 returns to 0 with the following trailing edge. FF_2 cannot be triggered again, nor can FF_1, because $\overline{Q}_1$ rises to 1 and stays there. The pulse output on Q_1 closely coincides with the trigger-pulse period, synchronizing the trailing edges. The trailing edge can therefore be used to change counter states or for other control functions.

Reset pulses must be noise-free and shorter than the trigger period if double triggering is not to occur and FF_1 is not to be locked in the on state. A circuit like the "noiseless" pushbutton shown will shape and clean up switch inputs. It normally operates from dc to 75 kilohertz, but can be extended to at least 1 megahertz by changing the RC timing network on the μL914 dual RTL gate.

The timing diagram shows what happens when reset pulses occur randomly. But if reset is periodic, the pulse-separator output will be periodic and the timing of the output pulse train will depend on the trigger and reset periods.

This circuit was developed through a research grant from the National Air Pollution Control Administration, Consumer Protection Environmental Health Service, Public Health Service.

More than a one-shot. Two flip-flops operating as a pulse separator (A) align reset pulses with a trigger pulse train. FF_1 cannot change state until FF_2 is reset and changes the state of J_1 and K_1. Then FF_2 triggers and causes FF_1 to return to the standby state. Applications include "noiseless" pushbutton control (B).



Bootstrap boosts gain of low-noise rf preamp

by R.J. Turner
Radio Corporation of America, Moorestown, N.J.

An easy way to improve the gain of a low-noise rf preamplifier while increasing bandwidth is to put a bootstrapped transistor between the input and output stages. The input stage can be operated at a higher load-resistance level, producing better gain and bandwidth due to the lower input capacitance of the output buffer.

The preamplifier shown has a gain of 20 decibels and a first stage designed for a bandwidth of 380 megahertz. Without the bootstrap connection between Q_3's emitter and Q_2's collector, the cutoff frequency is only 150 MHz, but with the the cutoff jumps to 275 MHz. The physical capacitance of Q_2's base is mostly C_{cb}. It is typically 0.5 picofarads but is reduced to an effective capacitance of less than 0.1 pF by the bootstrap action of C_1.

This method is useful in vhf receivers that need a low-noise, high-gain preamp to overcome losses when low-level signals are mixed or gated. The design will detect 5-microvolt signals, doesn't hang up on strong signals, and recovers in less than 50 nanoseconds from a 40-dB overload.

As usual, the gain-bandwidth tradeoffs are

gain $\approx \beta R_L$
bandwidth $= 1/(2 \pi R_L C)$

Here, beta is Q_1's high-frequency current transfer ratio, R_L its collector load, and C is Q_2's collector-base capacitance. The bootstrap divides C by $(1/1 - A_v)$. A_v is the voltage gain between Q_2's base and collector via Q_3's emitter. Typically, this gain is over 0.95.

Some compromises are needed if larger values of R_L are wanted at the input stage. Collector current has to be high enough to give good gain, but low enough to reduce shot noise.

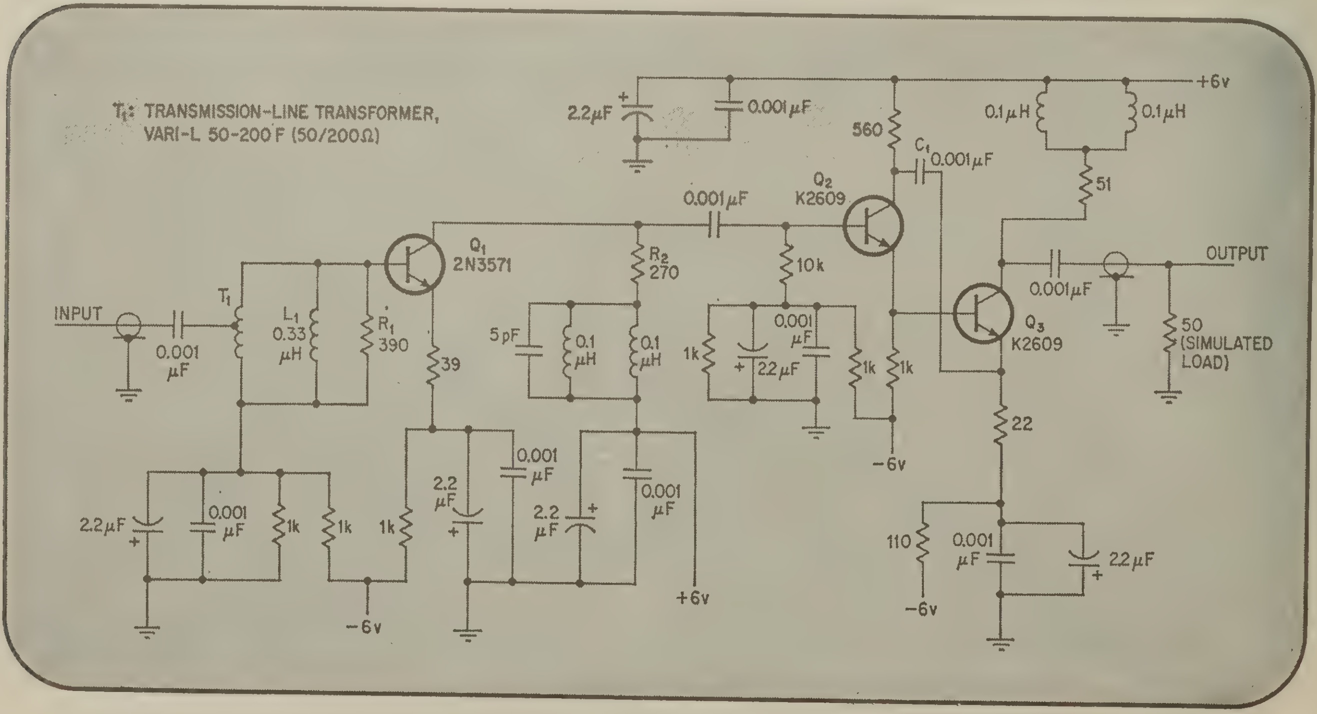
Also, it's desirable to have a high impedance looking into the base of Q_1, in order that a physical resistive termination may be used to provide a low input VSWR. (For this case R_1 equals 390 ohms.) The effective resistance appearing at Q_1's base should be 100 ohms for the optimum noise figure. But in practice, when a compromise must be made between noise figure and VSWR, and with Q_1's emitter biased at 2.25 milliamperes, this resistance is 130 ohms.

A toroidal, wideband transformer, T_1, transforms a 50-ohm input to an impedance of 200 ohms at the base of Q_1. Resistor R_1 and inductor L_1 are selected to optimize the input VSWR. R_1 is typically 390 ohms and L_1 0.33 microhenries.

The net result is a first-stage gain of 20 dB, a noise figure of 4.5 dB and a VSWR of less than 1.2 from 130 to 170 MHz.

Q_1 has enough feedback (emitter degeneration) to provide a first-stage bandwidth of 380 MHz. However, the shunt-peak networks on the collectors of Q_1 and Q_3 are tuned to 150 and 300 MHz, respectively, to keep the response flat within ±0.5 dB from 90 to 250 MHz. The corresponding 0.1-dB points are 100 and 200 MHz. Finally, the Q_2-Q_3 state isolates the input stage from a normal 50-ohm output load.

Low C, low noise. Low noise, large bandwidth, and low input VSWR are achieved by optimally loading input stage Q_1. Q_2's collector is bootstrapped from Q_3's emitter. This lowers the capacitance seen by Q_1 and allows gain or bandwidth to be increased.



High-voltage pulser spares battery supply

by W.J. Orr
National Research Council of Canada, Ottawa

A high-voltage one-shot will make its batteries last, thanks to a big capacitor and a small output duty cycle that enable it to time and generate pulses with large peak values while draining very little current. Pulse delays are variable between 0.5 and 20 microseconds.

The circuit is much more convenient to use in laser and plasma physics experimentation than line-powered pulsers and coaxial-cable delay lines. It can't upset instrument synchronization with line transients, and delay adjustment is easy.

Transistors Q_1 through Q_4 form a monostable multivibrator timed by R_1 and C_1. The multivibrator is triggered within 50 nanoseconds by dropping the input level to —3 volts. Zener diode D_1 is selected for the negative trigger level desired; a pulse-inverting transformer can be used for positive triggers. After Q_1 turns on, a 15-V step pulse is generated.

The pulse level is maintained by electrolytic capacitor C_2 until the current charging C_1 through R_1 drops enough to bring Q_2 out of saturation. On time is approximately $R_1C_1\ln(0.4h_{FE})$, where h_{FE} is Q_2's dc current gain. For this circuit, on time is 400 μs.

The voltage step across zener diode D_2 charges C_3 through R_2. When the current through R_3 reaches the peak-point current of tunnel diode D_3, the diode switches to its higher-voltage state. This saturates Q_5, releasing the charge stored in C_4 and triggering thyristor D_4. Thus, C_5 is discharged, generating the output pulse. The pulse has a rise time of 30 ns and peaks at more than 300 V when transformer T_1 is used. D_4 can switch 30 amperes in 30 ns.

C_3's charging slope (and therefore the time D_3 and Q_5 delay the pulse output from the trigger input) is adjusted by varying R_2. Delay time is

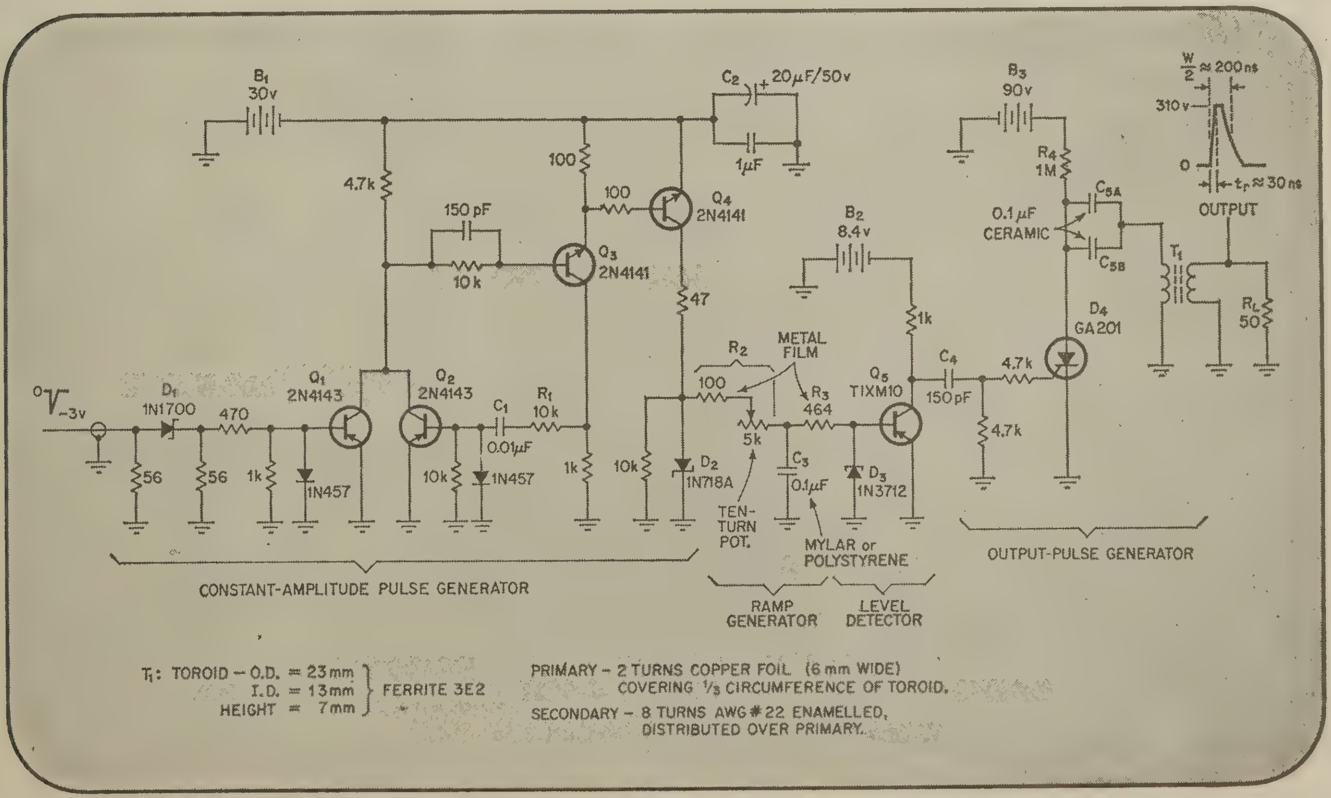
$$t_d \approx \frac{R_2 R_3}{R_2 + R_3} C_3 \ln\left[\frac{1}{1 - (R_2 + R_3) I_p/V_{zener}}\right]$$

where V_{zener} is 15 V and I_p is 1 milliampere for D_3.

The batteries mainly supply bias currents to their circuit stages during the pulse times; they recharge C_2, C_4, and C_5 during recovery times. C_2 gives up only a fraction of its energy in charging C_1 and C_3, so the recharging current from battery B_1 is low. C_4 is small and C_5 can be trickle-charged through a large resistor, R_4, keeping output pulse duty cycle (and therefore average dissipation) low.

On standby, the current drain is a mere 2 microamperes, due mostly to leakage of C_2 and Q_5. Timing jitter is within ±0.01 μs; temperature stability is excellent. A drop of 5 V in B_1 changes the delay only 0.05 μs at the 20-μs delay setting.

Delay generator. An input pulse triggers a sequence of charge transfers that delay and generate a high-voltage pulse output. C_1 pulls energy from C_2 to time the one-shot's basic period while C_3 charges through R_2 to set the pulse delay time. Then C_4 switches the thyristor to discharge C_5, which has been storing output pulse energy.



T_1: TOROID – O.D. = 23mm
I.D. = 13mm
HEIGHT = 7mm
} FERRITE 3E2

PRIMARY – 2 TURNS COPPER FOIL (6 mm WIDE) COVERING 1/3 CIRCUMFERENCE OF TOROID.
SECONDARY – 8 TURNS AWG #22 ENAMELLED, DISTRIBUTED OVER PRIMARY.

Probability analysis cuts power supply needs

by S. Gery and E. Drogin
AIL division, Cutler-Hammer Inc., Deer Park, N.Y.

The law of averages is on the side of the digital system designer who saves money on power supplies by not designing for the worst-case current requirement. That way, there's little chance that any large collection of digital devices will pull much more than the total of their average currents.

Risk can be limited to perhaps one blown fuse every few centuries by calculating a safety factor with probability statistics. The criteria are:

$$P = \text{probability that } I_s > I_{ave} + n\sigma$$

where

$$\sigma = \sqrt{K}\left[\frac{I_{max} - I_{min}}{2}\right]$$

and I_s is the supply current; I_{ave} is the average supply current; n is the probability factor (see table); σ is the standard deviation of current; K is the number of statistically independent devices; I_{max} is the maximum current of one device; and I_{min} is the minimum current of one device.

Once I_{ave} is found (it's simply $K(I_{max} + I_{min})/2$ for all similar devices), the safety factor can be reasonably approximated. A large K makes the statistical distribution of currents nearly normal, even in the "tails" of the $n\sigma$ curve. A conservative application of normal approximation is $K \geqq -30(\log_{10}P)$.

The value of n depends on the acceptable risk. For instance, at n = 9, the probability of an insufficient I_s is less than once in $10^{18.9}$ trials. A trial in a digital system is a clock period; if the clock frequency is 10 megahertz, there are 3.2×10^{18} clock pulses in 100 years, so I_s is statistically safe for three centuries.

Even the most conservative engineer might settle for a lower value of n, particularly at lower clock rates. For example, assume a system contains 600 gates operating randomly and that each gate needs 1/30th of an ampere in the 0 state and 10 milliamperes in the 1 state. If it is equally probable that each gate will be in the 0 or 1 state at any given time, $I_{ave} = 13$ A and $\sigma = 285$ mA. For n = 9, $I_s = 15.6$ A, which is more than 20% less than the worst-case requirement that 20 A (600/30) be supplied.

In practice, designers of large systems should consider how many devices pull more than the average current specified by the device manufacturer, rather than calculate σ with worst-case I_{max} and I_{min} values. Moreover, the 1 and 0 probabilities for a system may not be equal.

Frequently, one set of gates will switch to 1 when another set switches to 0, or vice-versa. Paired off, such gates don't need more than an average current increment, reducing the magnitudes of K and $n\sigma$. Moreover, functional blocks, such as flip-flops, have current requirements that are independent of state, also reducing K.

On the other hand, a "master clear" or similar control may switch large numbers of gates into fixed states. The equations don't change if the gates are held in I_{min} states, but I_s must increase if more gates switch into I_{max} than I_{min}.

Probability table*

n	$-\log_{10}P$
5	6.542
6	9.005
7	11.892
8	15.206
9	18.947
10	23.118

* From M. Abramowitz and I.A. Stegun, "Handbook of Mathematical Functions," AMS-55, Table 26.2, p. 972, National Bureau of Standards, June 1964.

Stable FET clamp operates at 10 MHz

by Tom E. Polcyn
Center for Research in Engineering Sciences, Lawrence, Kan.

In addition to handling video signals, a clamping circuit also can serve well as a general-purpose dc level restorer. It locks the level of its output to a reference voltage, following the timing of randomly arriving inputs out to frequencies of 10 megahertz. And unlike conventional dc restorers, its input impedance is high, output impedance is low, and temperature stability is good.

The standard diode-capacitor restorer often distorts signals, especially if the signal frequencies are random or, like video signals, contain very narrow pulses. Moreover, the circuit's output impedance is relatively high and the diode makes it temperature-sensitive.

For the video clamp, the capacitor C_1 blocks off the original signal level. But the input pulse is replaced by one at V_{ref} for the duration of the pulse time.

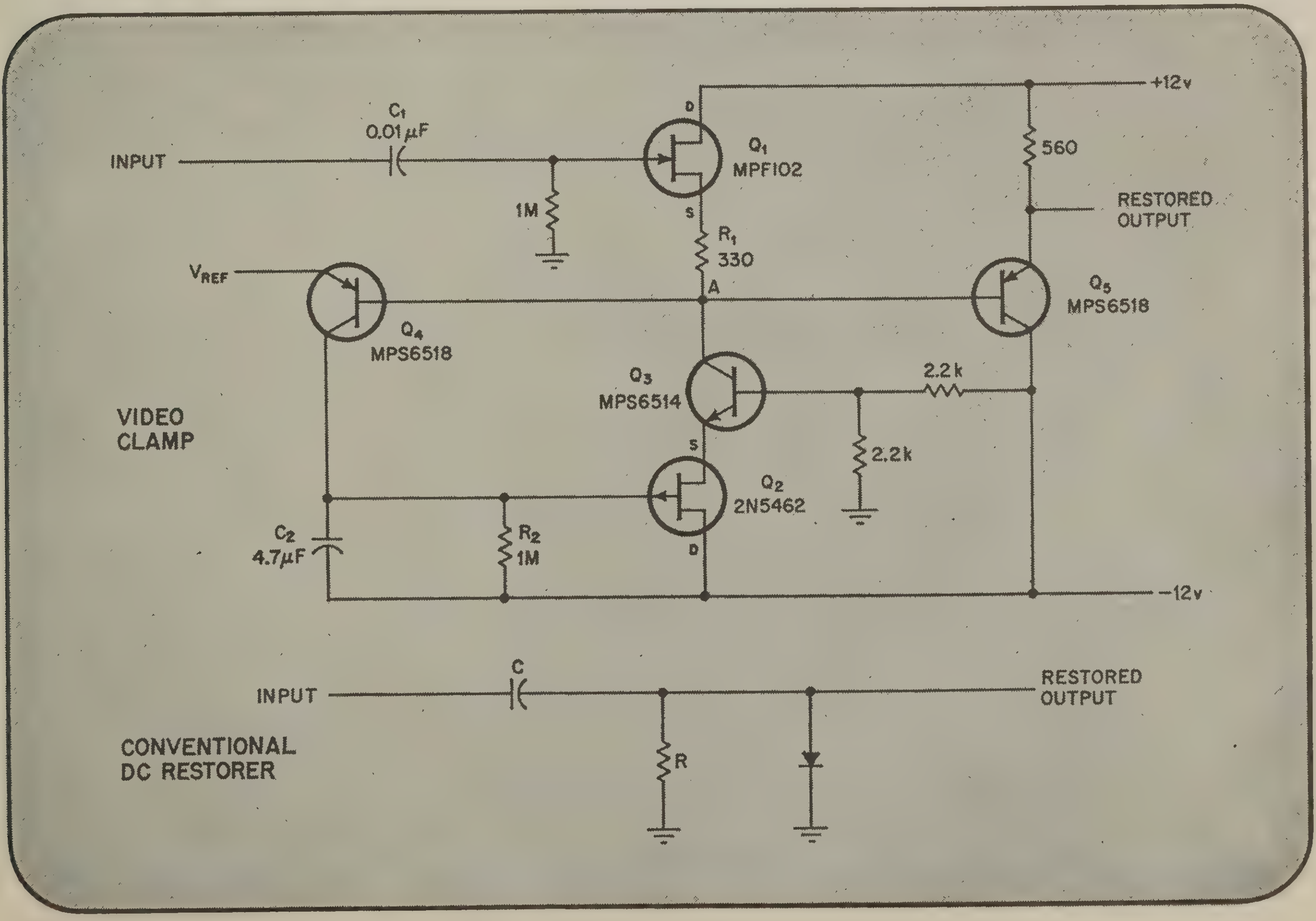
A second FET, Q_2, acts as a constant-current source for Q_1 and R_1 through Q_3, which is cascode-connected. The gate-to-source voltage of Q_1 and the voltage drop across R_1 also are constant while the circuit is quiescent.

When a pulse is ac-coupled through C_1 to the gate of Q_1, the original dc component is lost. As a result, the signal reappears at point A with a different dc level. This level tries to go toward —12 volts but as soon as it is 0.6 V below V_{ref}, Q_4 turns fully on and C_2 begins to charge positively.

Because Q_3 has been maintaining a constant voltage at the source of Q_2, the gate-to-source voltage of Q_2 now increases as C_2 charges. Q_2 must reduce the current it supplies to Q_1 and R_1. The voltage now increases at point A, reducing the collector current of Q_4 and the charging of C_2.

Resistor R_2 and capacitor C_2 are chosen so that C_2 discharges very slowly when Q_4 turns off. For a fraction of the time constant R_2C_2, the current will remain nearly constant in Q_1, Q_2, Q_3, and R_1. Therefore, the most negative value of the signal at point A is clamped about 0.6 V below V_{ref}. The emitter-follower action of Q_5 shifts the signal back up about 0.6 V so that the output voltage is effectively clamped to V_{ref}. Temperature drift is negligible if Q_4 and Q_5 are well matched.

Clamping at 10 MHz. Current and voltage at point A are constant. Q_4 turns on and C_2 charges, making Q_2 reduce the current through Q_1 and R_1. Then Q_4 cuts off and C_2 slowly discharges. This action clamps point A at 0.6 volt below V_{ref}. Q_5 then shifts the output level up by 0.6 V to V_{ref}.



Impedance-lowering op amp speeds filter response

by Robert J. Battes
Delta-Pacific Electronics, Prospect Heights, Ill.

By minimizing ac impedance, an active filter will solve the problem of removing ripple from dc signals applied to digital voltmeters and other equipment with high input impedances.

Simple RC filters are not very practical in such applications because a large capacitor is needed to attenuate the ripple. Such a large capacitor can stretch out the response time, while its leakage current will heavily load the dc signal. But by lowering just the ac impedance, the necessary capacitance will be kept small while attenuation will improve over a wide range of ripple frequencies.

Ripple at point A is coupled through dc blocking capacitor C_1 to the operational amplifier, which inverts and greatly amplifies the ripple. Because the negative feedback, which is brought back to point A through C_2, is large, the effective ac input impedance is reduced at point A by about X_{C2}/A_V. This is the ratio of C_2's reactance to the voltage gain from A to B when C_2 is disconnected.

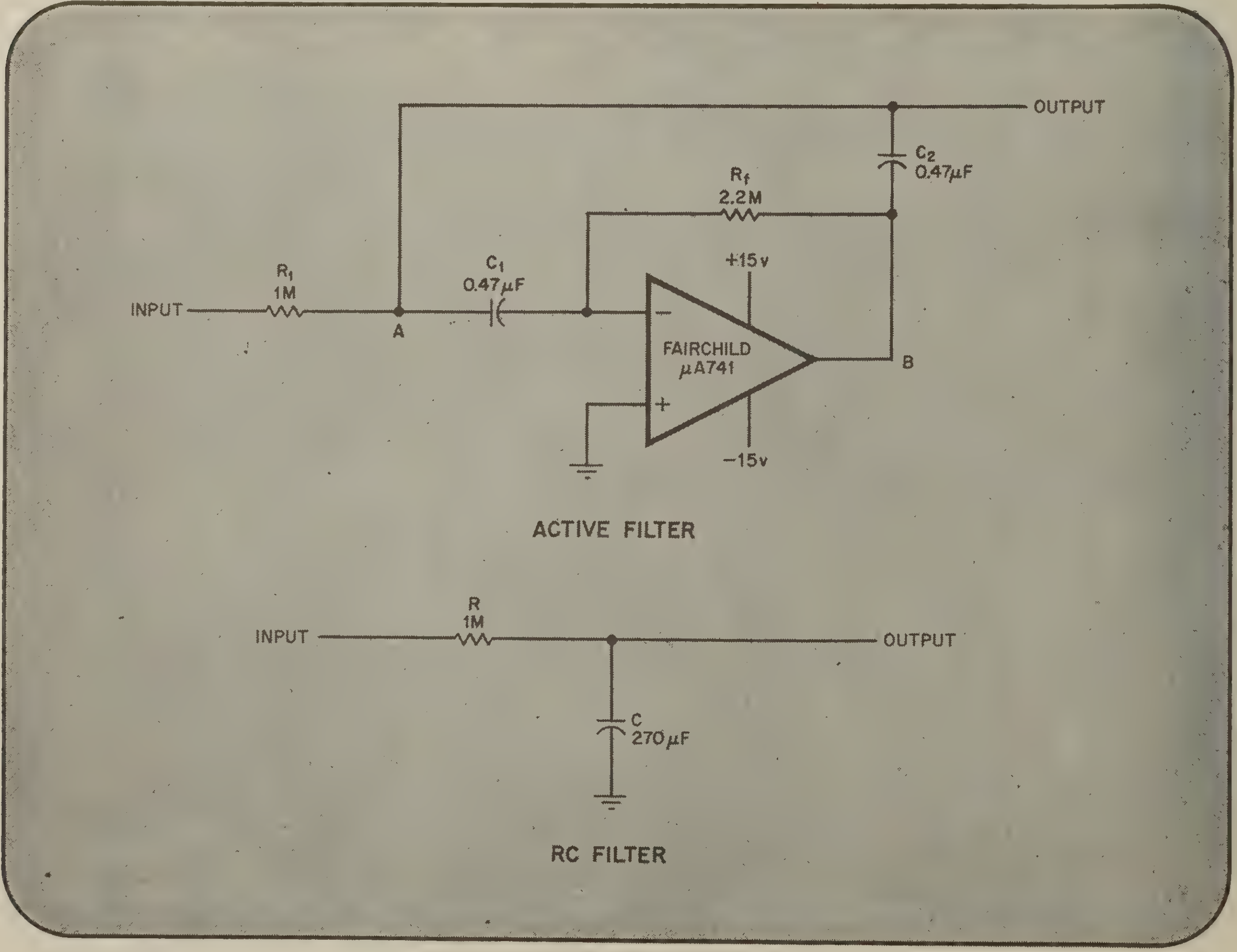
As a result, the ripple at A drops by nearly A_vR_1/X_{C2}, or more than 100 decibels at 60 hertz. It is easily attenuated by small, low-leakage capacitors that also isolate the dc signal line from the amplifier bias currents.

Attenuation remains high well into the audio region. Both X_{C2} and A_V drop rapidly as frequency rises. The fall in A_V is due to the amplifier's internal frequency-compensating components.

The active filter takes about 5 seconds to bring the output to within 1% of final value after a step change in the dc level. The passive network, which attenuates about 100 dB at 60 Hz, takes some 1,350 seconds.

In addition, the active filter maintains a good response speed as frequency increases into the line and audio regions.

Capacitance amplifier. Ability of small capacitors to attenuate ripple is multiplied by inverting, amplifying, and feeding back the ripple to the signal input. This reduces the effective ac impedance by the ratio of C_2's reactance to the amplifier gain. A passive filter responds slowly because a large capacitor is needed to attenuate directly.



Hitch in time saves gates in 12-hour digital clock

by Vernon R. Clark
Applied Automation, Inc., Bartlesville, Okla.

The trickiest task in designing a 12-hour digital clock is decoding the hours-counter outputs. As the truth table shows, a binary number sequence cannot directly control this section.

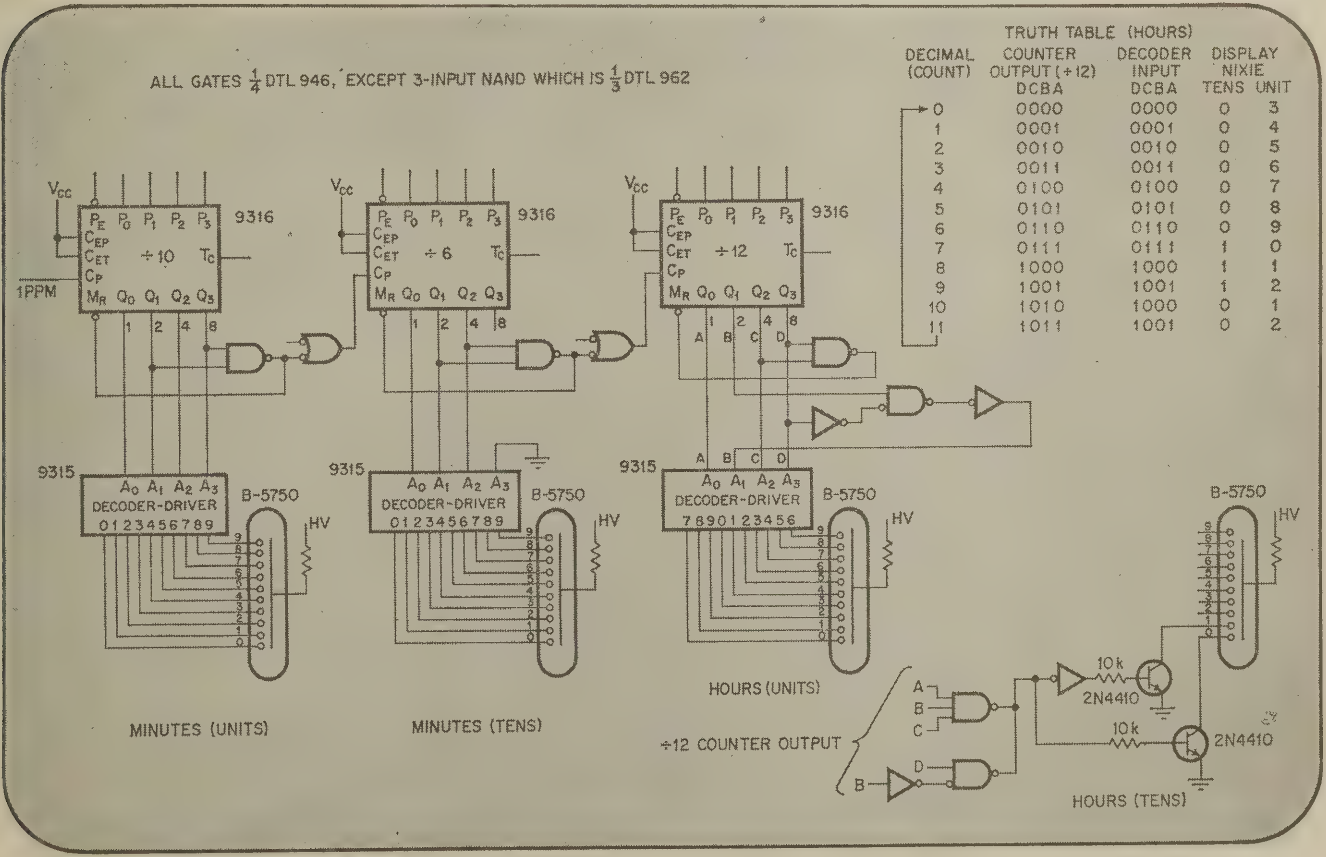
The hours (units) logic can be unsnarled with only three gates—three-fourths of a DTL 946 quad NAND package—after rearrangement of the Nixie tube connections to the third decoder-driver.

To advance the counter output by three hours, decoder output 0 is connected to cathode 3, output 1 to cathode 4, etc. Then the three gates can make the decoder's B input go low by inhibiting B whenever D is high. The decoder reads counts 10 and 11 as 8 and 9 counts, so the hours (units) cathodes light in 1, 2, 1, 2, order before the counter resets and the clock goes to 3 o'clock.

Decoding the hours (tens) merely requires gating that enables cathode 1 of the hours (tens) Nixie when counter outputs ABC = 111 while D is low, and when D is high then B is low. The 2N4410 transistors are high-voltage drivers for the hours (tens) Nixie. The 900 DTL cannot drive the cathodes directly because their output transistors can't handle the high voltage.

The 12-hour digital clock was designed for a computer application and is applicable to other timing functions as well as timepieces. To tick off seconds, two more 9316s, connected like the minutes counters but with a one pulse per second input, can be added at the left. The divide by 6 and 10 counters could have been used to divide down from a 60-hertz reference source. Parallel setting and resetting, and a.m. and p.m. indication also can be worked in.

Ten equals 12 hours. Rearranging the hours-display connections simplifies hours decoding. The gating makes hours 1 and 2 repeat by holding decoder input B low when input D is high, as shown in the truth table. Hours tens are decoded by sensing when D is high and B is low, or when D is low and ABC are high.



TRUTH TABLE (HOURS)

DECIMAL (COUNT)	COUNTER OUTPUT (÷12) DCBA	DECODER INPUT DCBA	DISPLAY NIXIE TENS	UNIT
0	0000	0000	0	3
1	0001	0001	0	4
2	0010	0010	0	5
3	0011	0011	0	6
4	0100	0100	0	7
5	0101	0101	0	8
6	0110	0110	0	9
7	0111	0111	1	0
8	1000	1000	1	1
9	1001	1001	1	2
10	1010	1000	0	1
11	1011	1001	0	2

Low-cost exclusive-OR needs no power supply

by K.D. Dighe
K & M Electronics Co., Baltimore, Md.

An exclusive-OR gate with three resistors, two low-power, small-signal npn transistors, and no external power supply could hardly be simpler. And by adding an inverter, the exclusive-OR gate becomes a coincidence detector.

Conventional exclusive-ORs take four or five gates and a logic supply. Other discrete-component designs with fewer than four or five gates require positive and negative supplies or circuitry to split a single supply.

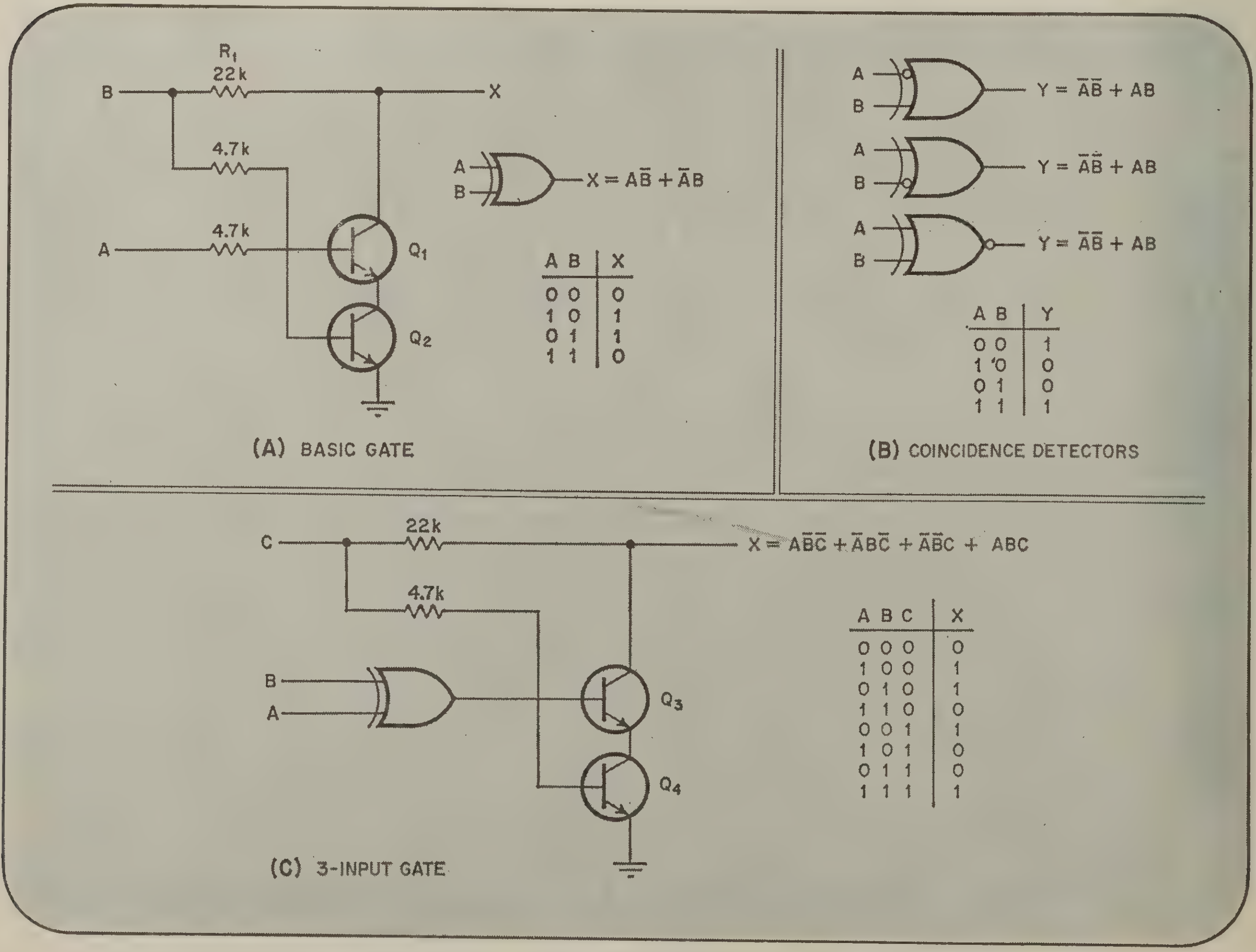
However, in this circuit, input signals operate the gate and drive the load. When low-voltage signals are applied to both of the basic gate inputs, both transistors are off and the output is low. A high voltage on both inputs turns both transistors on, but the output is still low because the two saturation drops pull Q_1's collector down to 0.4 volt.

If input A is high and B is low, Q_1's base-emitter diode opens and its base-collector junction is forward-biased. The output is high and the load is driven through the latter junction. When A is low and B is high, the load is driven by the voltage through resistor R_1. Now the base-emitter junction of Q_2 is forward-biased, but Q_1 is off and does not draw current.

Therefore, the exclusive-OR function $X = A\overline{B} + \overline{A}B$ is provided with positive logic assignments to the inputs and output (low voltage is 0 and high voltage is 1). Mixed positive and negative inputs or inversions as in diagram B change the gate to a coincidence detector with the function $Y = \overline{AB} + AB$.

Extended with a second stage (diagram C), the gate provides $X = A\overline{BC} + \overline{A}B\overline{C} + \overline{A}\overline{B}C + ABC$. Or with an inverter, the output becomes $Y = \overline{ABC} + AB\overline{C} + A\overline{B}C + \overline{A}BC$. Configuration C gives a high output when any one or all of its inputs are high. For any other condition, the output is low.

Signal-powered logic. A high logic signal on the A or B input drives the load through Q_1 or R_1. Two low inputs or two high inputs hold the output low. So the basic gate (A) is an exclusive-OR. An inverter makes it a coincidence detector (B). Two stages can handle three inputs (C).


R_1
22k
B
X
4.7k
4.7k
A
Q_1
Q_2
A
B
$X = A\overline{B} + \overline{A}B$
(A) BASIC GATE
A
B
$Y = \overline{A}\overline{B} + AB$
A
B
$Y = \overline{A}\overline{B} + AB$
A
B
$Y = \overline{A}\overline{B} + AB$
(B) COINCIDENCE DETECTORS
C
22k
4.7k
B
A
Q_3
Q_4
$X = A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C + ABC$
(C) 3-INPUT GATE

A	B	X
0	0	0
1	0	1
0	1	1
1	1	0

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	1

A	B	C	X
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

High-voltage amplifier offers high frequency, too

by Walter A. Cooke
Lockheed Missiles & Space Co., Sunnyvale, Calif.

Both high voltage and high frequency are hard to obtain in one amplifier. But if a common-base voltage amplifier is added to a low-voltage operational amplifier, both features can be achieved—and with excellent stability. The circuit can be used as a CRT cathode driver that delivers 50 volts, peak-to-peak, has a response of 10 megahertz, and is stable beyond 100 MHz.

Ordinarily, the high junction capacitance of a device with a high breakdown voltage imposes a low frequency response. But because of the common-base connection of the output stage, the design does not have to fight both the laws of solid state physics and Nyquist's response rules.

A common-base transistor gives only voltage gain, not current gain, and can operate with a small collector resistor. Its response is high because frequency rolloff is inversely proportional to collector resistance. And additional help is provided by the higher collector current, which raises cutoff frequency, up to a point.

The first stage is a high-frequency, high-current, hybrid amplifier, A_1. It must handle the load current, but its output need swing only 2.5 V pk-pk, at midfrequency since the common-base stage's gain is nearly 20.

A_1's inner-loop capacitance, C_1, is adjusted for system stability. It should roll off A_1's gain by 20 decibels per decade from dc to 10 MHz. Gain is then unity until rolloff resumes again at about 350 MHz. Making R_1 equal to R_2 balances the output swings of A_1.

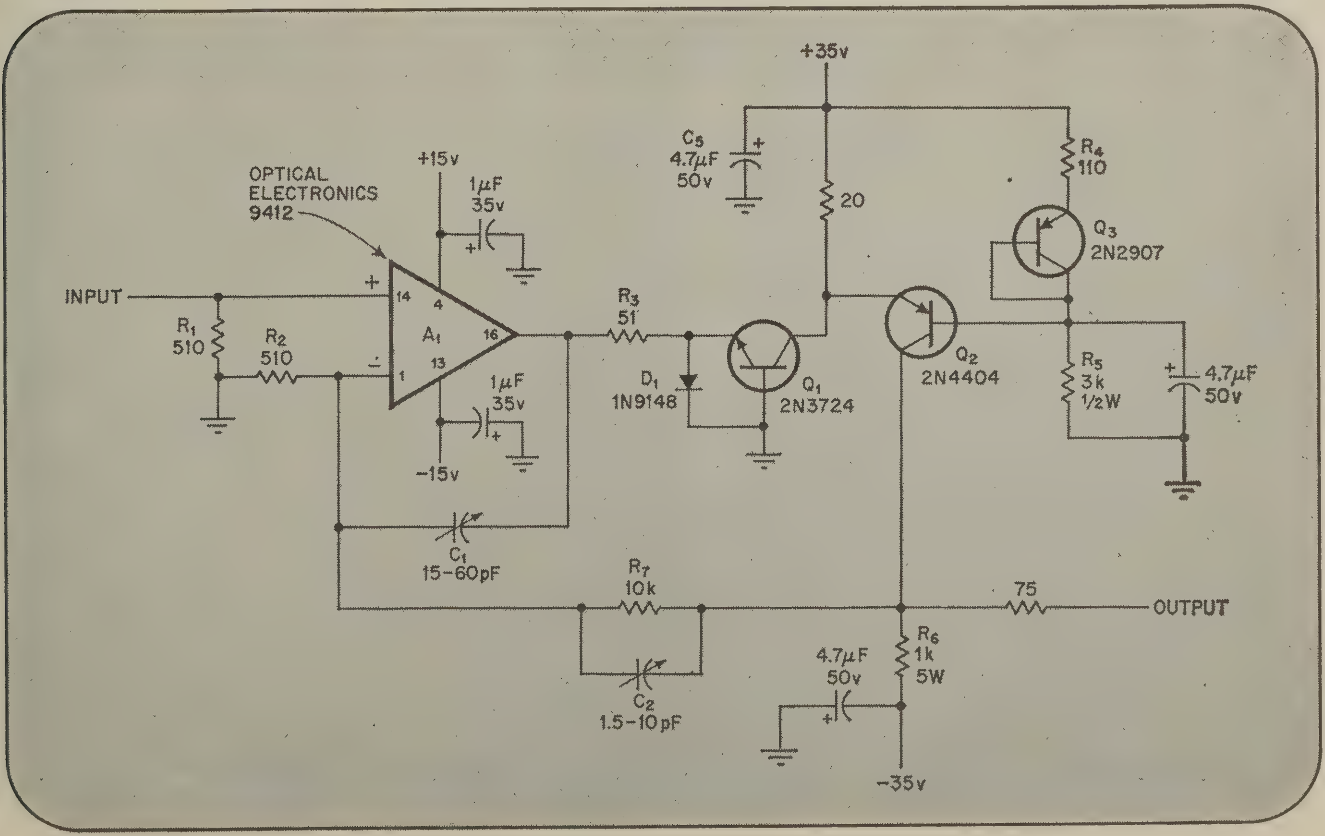
The amplifier's output controls Q_1 through resistor R_3 and diode D_1. Q_1 then translates this output up to the emitter of Q_2, which is biased near the + 35-V supply by R_4, R_5, and Q_3. The circuit's output swings symmetrically about the ground reference.

Second-stage voltage gain is approximately R_6/R_3 (19.6 for this case) from dc to 10 MHz. Rolloff to this point is controlled by A_1. At about 10 MHz, R_6 and Q_2's collector-to-base capacitance take over, also rolling off gain at 20 dB/decade.

Composite closed-loop gain is flat to 10 MHz; gain is about $1 + R_7/R_2$. Since A_1 inverts, making R_7/R_2 equal to R_6/R_3 keeps output overshoot small. Any overshoot can be damped by adjusting C_2. Open-loop gain is 77 dB from dc to about 30 kilohertz. It then rolls off at 20 dB/decade to zero crossover at 200 MHz, assuring closed-loop stability.

Q_1 and Q_2 must be heat-sinked and Q_3 should be thermally coupled to Q_2 to maintain the operating point during temperature changes.

Two-stage rolloff. Common-base connection of Q_2 allows its collector resistor, R_6, to be small. This prevents collector-to-base capacitance from rolling off voltage gain until signal frequency is 10 MHz. Below 10 MHz, the first stage rolls off until A_1 becomes a unity-gain amplifier. The two-stage rolloff keeps the entire amplifier stable.



Active RC network has two movable zeros, fixed poles

by Robert D. Guyton
Mississippi State University, State College, Miss.

An active RC network allows its zero locations to be placed anywhere in the complex plane, including positions on the positive real axis. Zero-pair locations can be moved over a circular path in the plane by varying the feedback resistance, R_f. The pole-pair position, however, remains fixed because, as the network's transfer function shows, it does not depend on R_f.

The basic circuit can be easily modified and adjusted for specific filter applications and also can be used as a compensating network in feedback systems—for example, the 60-hertz notch filter shown has a rejection of more than 70 decibels. Its zero-pair motions with variations in R_f can be seen in the pole-zero plot.

That the zeros will move as shown is clear from the general form of the transfer function:

$$\frac{E_2}{E_1} = \frac{R_3}{R_2 + R_3}\left[\frac{1 + s(R_1C_1 + R_2C_2 - R_2R_fC_1/R_3) + s^2R_1R_2C_1C_2}{(1 + sR_1C_1)[1 + sR_2C_2R_3/(R_2 + R_3)]}\right]$$

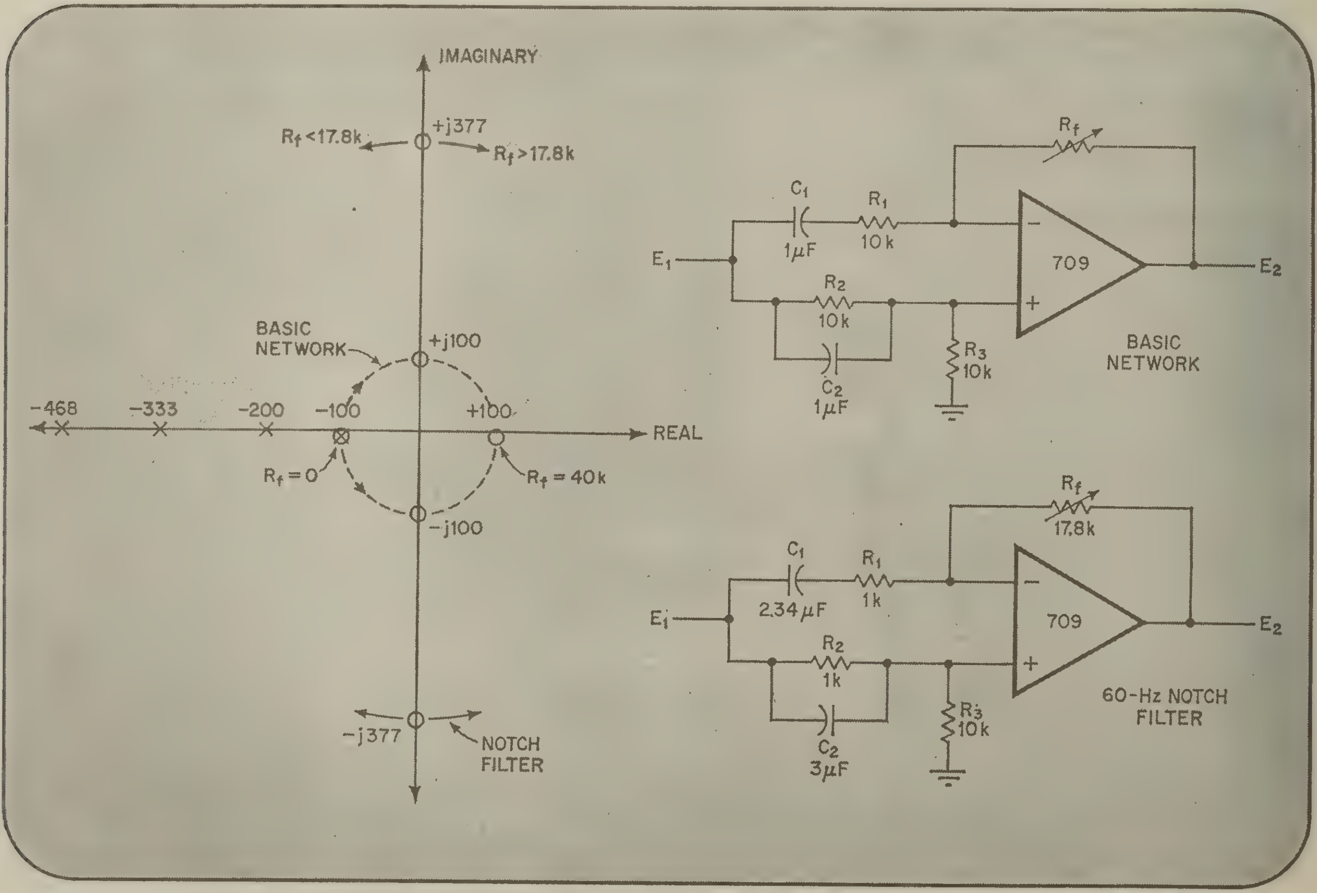
For the basic network, with R_f in megohms, the function reduces to:

$$\frac{E_2}{E_1} = \frac{1}{2}\left[\frac{1 + s(0.02 - R_f) + s^2 \times 10^{-4}}{(1 + 0.01s)(1 + 0.005s)}\right]$$

At $R_f = 0$, the two zeros are on the negative real axis at −100. As R_f increases to 20 kilohms and then to 40 kilohms, the zeros move to a complex pair at ±j100 and then a pair on the positive real axis at +100. The poles remain fixed and real at −100 and −200.

Changing the fixed RC values will alter the path radius. The 60-Hz notch filter has a complex pair of zeros at ±j377 with a nominal R_f of 17.8 kilohms. The value of R_f is determined by experimental adjustment. The poles, in this case, remain fixed at −333 and −468.

Variable filter. Pole-zero plot shows circular motion of zero pair in an active RC circuit with variations in the feedback resistance, R_f. The circuit can perform a specific filtering function or can act as a compensating network in feedback systems. Basic network motion is in color and adjustment of notch filter is in black.



Any voltmeter reads electronic thermometer

Robert J. Battes
Delta-Pacific Electronics, Prospect Heights, Ill.

A silicon-diode probe and an operational amplifier with an unusual gain adjustment are the key elements in an electronic thermometer that gives a readout, in degrees, on an ordinary voltmeter. The sensing circuit's voltage variations can be adjusted to align with a temperature scale. For instance, a 10- or 100-millivolt reading can represent 1°C at one setting or 1°F at another setting of the amplifier.

The op amp is connected as a differential amplifier. An input that varies with the temperature of probe D_1 is obtained through resistor R_1 and part of R_2. Zener diode D_2 and R_3 provide a reference voltage; offset is adjusted by R_4. R_2 is the gain adjustment, but it is not entirely within the feedback path as shown on the diagram of the conventional differential amplifier. In the location used, R_2 helps to make the output both linear and scalable.

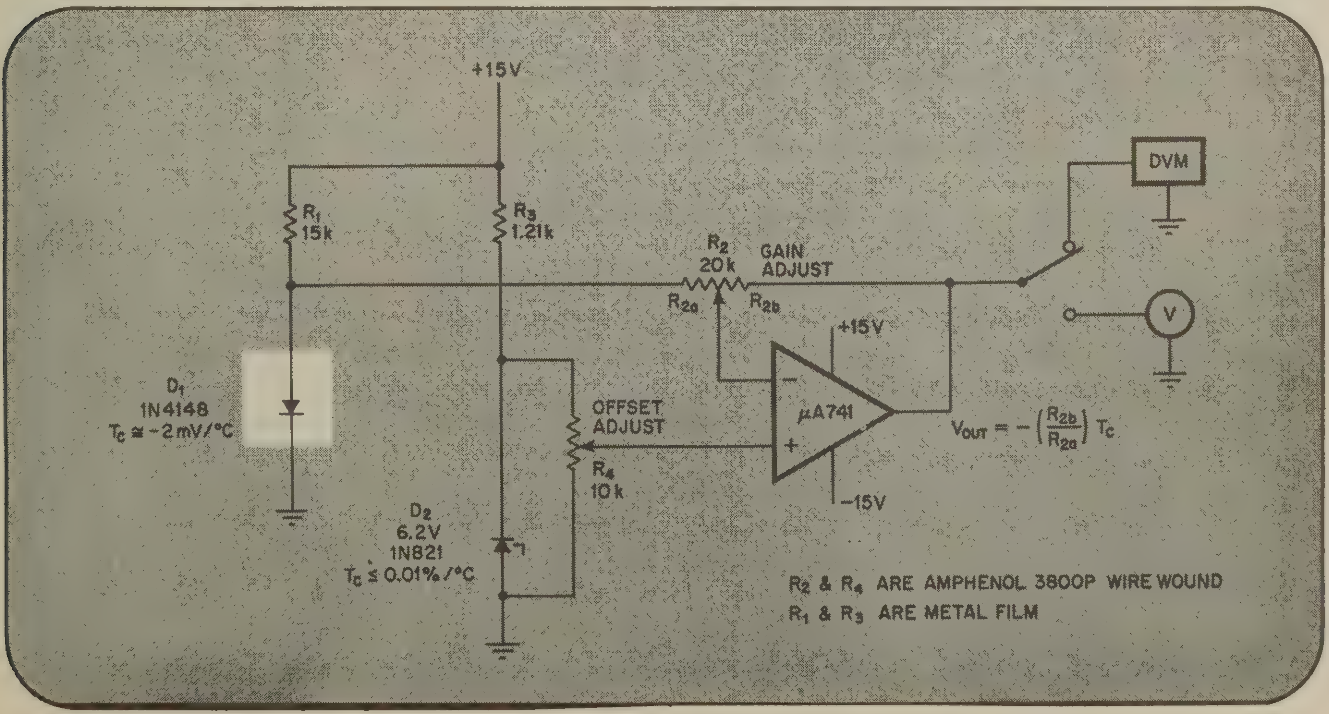
The values of R_1, R_3 and R_4 do not significantly affect the gain of the amplifier. The low impedance of the zener diodes, about 25 ohms, swamps out the presence of R_1 and R_3, and the high impedance of the amplifier masks the presence of R_4, which is much lower in value. The output voltage can be expressed in terms of R_2 and the temperature coefficient, T_c, of D_1.

$$V_{out} = -(R_{2b}/R_{2a})\,T_c$$

After potentiometer R_2 in the actual circuit is adjusted to bring the output within a suitable range on the voltmeter, potentiometer R_4 is used to adjust offset. This aligns V_{out} with the desired temperature scale so that the reading corresponds to degrees without further conversion. The instrument is calibrated by setting R_4 with the probe at a known temperature to calibrate the instrument.

Metal film resistors, wirewound potentiometers, and the small temperature coefficient of the temperature-compensated zener diode give the circuit excellent temperature stability. Minor variations in supply voltages do not significantly affect accuracy. Since the dynamic impedances of the two silicon diodes are matched closely, supply voltage changes result in a common-mode input signal that is greatly attenuated by the amplifier.

Volts by degrees. Amplifier adjustments allow the temperature of probe D_1 to be read on the voltmeter without further scaling or conversion factors. The output is scaled with R_2, which is located to simplify scaling by contributing to R_1. Adjusting offset with R_4 allows voltage to represent degrees F or C.



Low-voltage feedback loop controls high-voltage supply

By Roy J. Krusberg,
University of Georgia, Athens, Ga.

Considerable savings in size, cost, and complexity can be achieved by limiting the current in the primary winding of a high-voltage power supply's transformer, instead of controlling the output from the secondary winding. Much of the regulation circuitry can be built with low-voltage components, reducing cost and bulk, and eliminating sticky decoupling problems.

This approach is illustrated by a photomultiplier tube supply whose output ranges from 500 volts to 3.5 kilovolts, at currents up to 1 milliampere. Regulation can be as tight as 0.001%.

Q_1, a power transistor suitable for 117-volt operation, is located in the direct-current arms of a full-wave rectifier between isolation transformer T_1 and high-voltage transformer T_2. A feedback current through two low-voltage operational amplifiers, A_1 and A_2, varies Q_1's gain. Current through the primary winding drops when the output voltage rises above a level selected with the taps on resistors R_1 through R_{17}, or rises when V_{out} drops below the selected level.

As A_2 drives Q_1 toward saturation or cutoff, T_2's output fluctuates about the desired output. Diodes D_5 and D_6 rectify the controlled high voltage ac signal while L_1 and C_1 filter the ripple to provide a smooth dc voltage output. The series-parallel resonant circuit filters better than a pi-section filter alone.

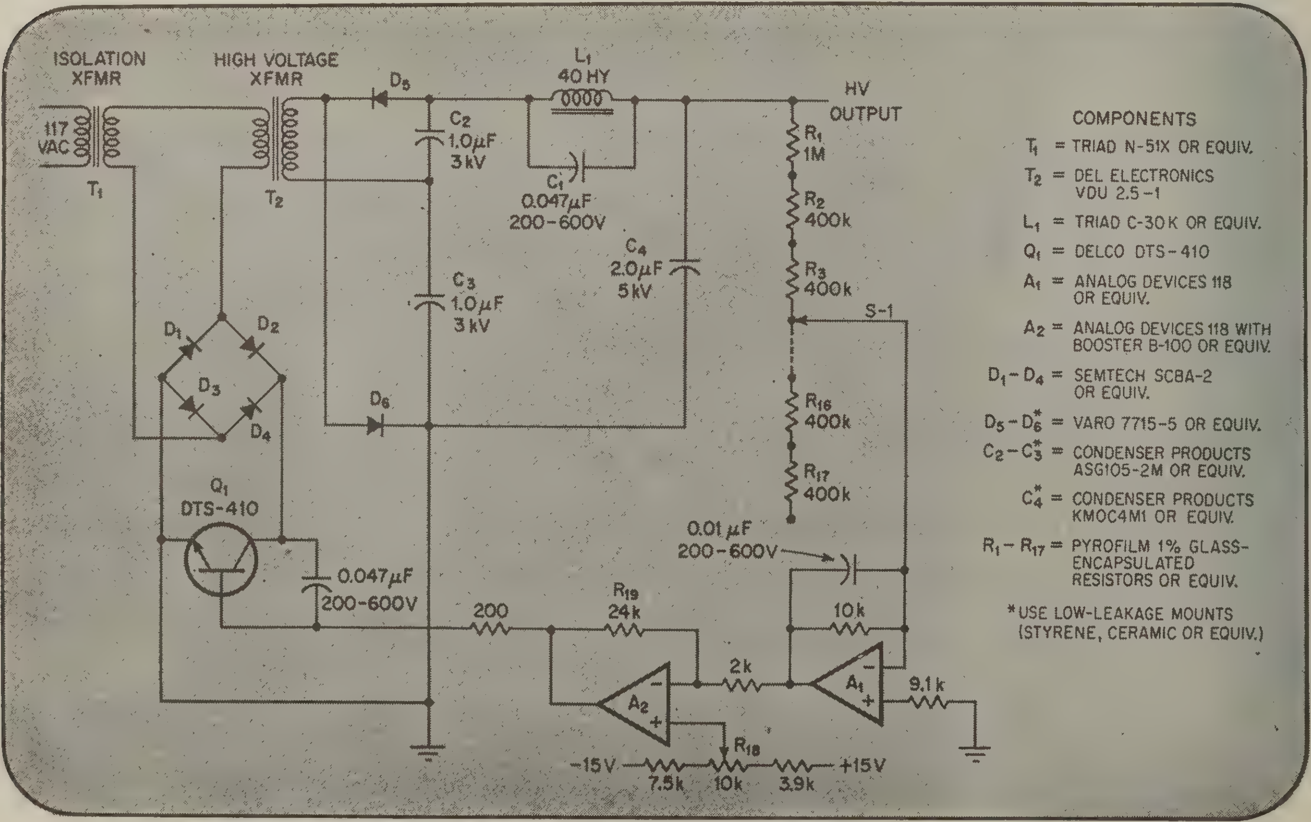
An offset voltage is injected into A_2's noninverting input to initially bias Q_1; current sources are the op amp power supplies and R_{18}. A_2's gain is set by feedback resistor R_{19} and is trimmed by R_{18} to give the desired output range in combination with the taps on R_1 through R_{17}.

After startup, the current sample obtained from R_1 through R_{17} feeds into A_1's inverting input. A_1 is connected as an inverting current amplifier; its output varies to hold the potential at the input summing point at zero. Since A_1's output is coupled into A_2's inverting input, the latter's polarity is suitable for driving Q_1.

If component values are changed, the standoffs must be adequate to isolate the low-voltage devices from ground. C_1 should be selected to resonate at 120 hertz with L_1. Tap resistors should be high-voltage glass-encapsulated types.

Because of its simplicity and reduced noise, a power transistor is preferred over a Triac and phase-control circuit for low-power regulation. Also, Triacs seem to have an erratic firing point, which degrades short-term regulation.

Volts control kilovolts. Current samples taken from the high-voltage output of power transformer T_2 are fed back through operational amplifiers A_1 and A_2 to control conduction in power transistor Q_1. The feedback limits the current in the transformer primary to regulate the secondary voltage, which is then filtered by L_1C_1.



COMPONENTS

T_1 = TRIAD N-51X OR EQUIV.
T_2 = DEL ELECTRONICS VDU 2.5-1
L_1 = TRIAD C-30K OR EQUIV.
Q_1 = DELCO DTS-410
A_1 = ANALOG DEVICES 118 OR EQUIV.
A_2 = ANALOG DEVICES 118 WITH BOOSTER B-100 OR EQUIV.
D_1-D_4 = SEMTECH SCBA-2 OR EQUIV.
$D_5-D_6^*$ = VARO 7715-5 OR EQUIV.
$C_2-C_3^*$ = CONDENSER PRODUCTS ASG105-2M OR EQUIV.
C_4^* = CONDENSER PRODUCTS KMOC4M1 OR EQUIV.
R_1-R_{17} = PYROFILM 1% GLASS-ENCAPSULATED RESISTORS OR EQUIV.

*USE LOW-LEAKAGE MOUNTS (STYRENE, CERAMIC OR EQUIV.)

Op amp's current booster ends crossover distortion

By J. Rodney Cox
U.S. Naval Ordnance Station, Louisville, Ky.

A high-performance operational amplifier's linearity usually suffers when output current is boosted. Adding a conventional power amplifier stage also adds crossover distortion for a fast changing signal. This can be prevented by adding a complementary power stage that conducts before a fast-changing signal crosses zero voltage. This booster stage also can improve slew rate.

The booster's two diodes, D_1 and D_2, establish a voltage offset that enables transistors Q_1 and Q_2 to go into conduction early. Q_1 starts boosting positive-going amplifier outputs as they drop near zero; Q_2 does the same for negative-going signals approaching zero. The booster output thus follows the signal waveform without the usual push-pull delays.

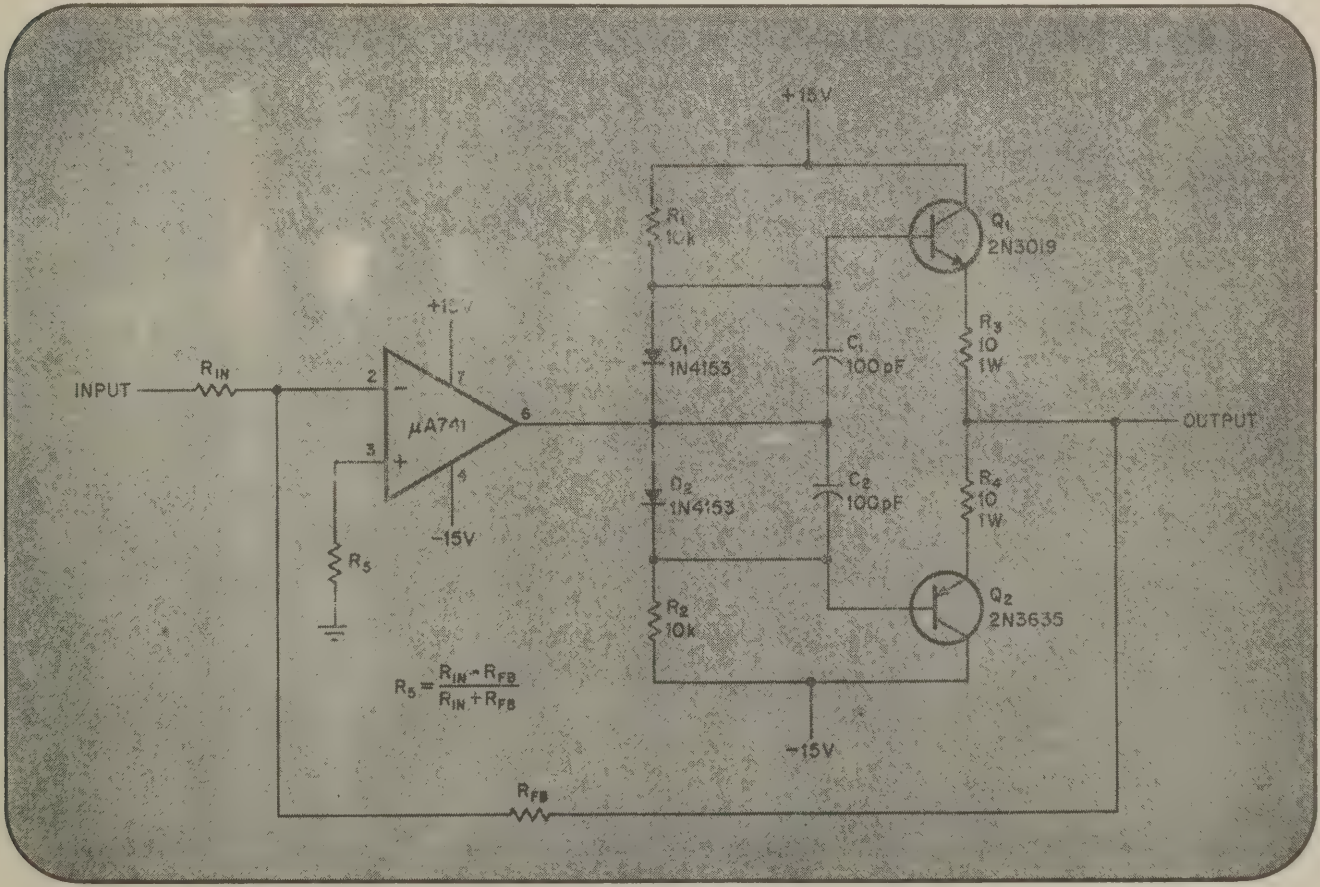
The transistors are biased to maintain small collector currents. On the Q_1 side, bias current comes in through resistor R_1 and splits between D_1 and Q_1. Q_2's complementary current flows out through R_2. The diodes provide a voltage offset so that no crossover is necessary before Q_1 and Q_2 conduct. Capacitors C_1 and C_2 preserve waveform integrity during fast signal transitions. Emitter resistors R_3 and R_4 prevent thermal runaway of the transistors.

Feedback is taken from the booster output to maintain the waveform through both stages. When accomplished through a conventional booster, it accentuates the distortion. Here, it doesn't.

The presence of the power stage in the feedback path increases slew rate. A monolithic op amp's slew rate is limited primarily by the fact that the amplifier's own output stage delivers current with internal negative feedback. Using the external power stage virtually eliminates capacitive feedback, speeding up the monolithic circuit's response.

The booster shown presents an output load of slightly less than 5 kilohms to the op amp. Minimum current gain of the transistors is 30. Output current rating of a typical high-performance amplifier such as the μA741 is 25 milliamperes. The booster increases this to about 500 mA; currents up to 300 mA undistorted were measured using the μA741.

High current, low distortion. Booster eliminates output crossover distortion by placing its transistors in conduction before the signal voltages cross zero. The diodes maintain a voltage offset so that a small current flows through the transistors. Also, the external booster minimizes capacitive feedback from the amplifier output, which raises the op amp slew rate.



Gate suppresses pulses from switch contact bounces

G. Fontaine
College de France, Paris

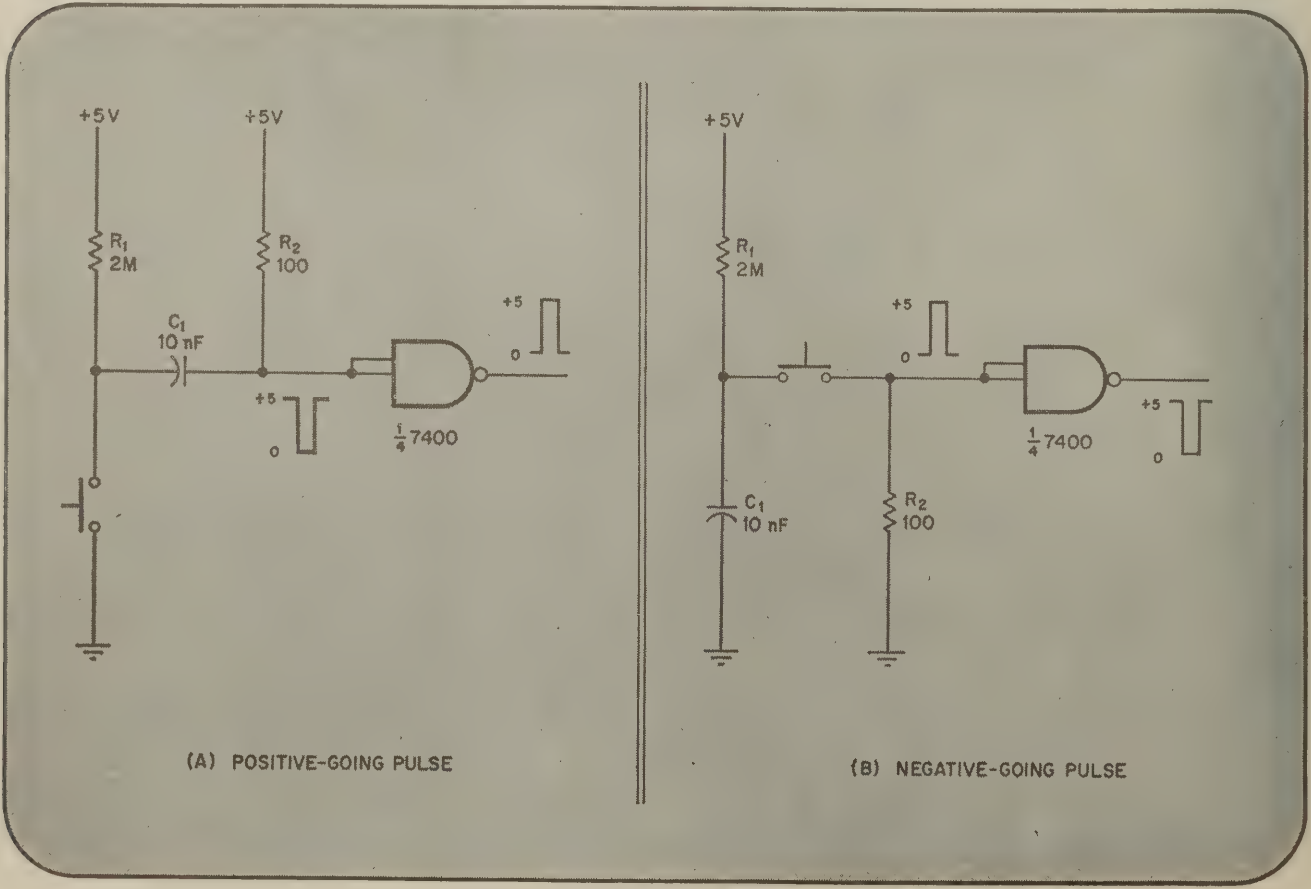
A gating circuit with an intrinsic dead time of 20 milliseconds will prevent switches from generating more than one logic pulse regardless of contact bounce. Most mechanical switches bounce anywhere from 5 microseconds to 5 milliseconds after the first closure.

Either circuit sets the pulse and bounce-suppression times via two resistors and a small capacitor. One circuit gives a positive-going output pulse and the other a negative-going pulse. Time constants are R_1C_1 for dead time and R_2 C_1 for pulse onset. The time constant for pulse onset is 1 microsecond with the values shown.

When the switch is open, circuit (A), C_1 is discharged since its plates are at 5 volts. The NAND gate input is high and its output is low. When the switch closes, the capacitor charges through R_2 in 1 microsecond. Current through R_2 lowers the gate input to 0 V, so the output goes to 5 V. When the first bounce arrives several microseconds later, C_1 is fully charged and the bounce has no effect. Subsequent bounces also are nullified until C_1 is discharged through R_1, which takes 20 milliseconds. By this time, the switch contacts are firmly closed.

In circuit (B), with the switch open, C_1 charges to 5 V through R_1 and the gate output is at 5 V. The input to the gate rises immediately to 5 V when the switch is closed, and the output drops to 0 V. C_1 then discharges through R_2 and charges through R_1 to complete the output pulse. All bounces are nullified until C_1 again charges through R_1.

Noiseless switching. A switch closure in circuit (A) charges C_1 through R_2, raising the gate output. Contact bounces cannot cause another pulse because C_1 requires 20 milliseconds to recharge through R_1 and set up the gate for another pulse. Circuit (B) provides the same suppression time by discharging C_1 and charging it slowly.



Feedback amplifier speeds phototransistor's response

by Michael L. McCartney
University of Virginia, Charlottesville, Va.

When difficulty is encountered in detecting low-level ac or pulsed light signals, the problem usually isn't a lack of sensitivity in the phototransistor. More likely it's a loss of bandwidth in conventional photocurrent-to-voltage converters.

One solution is to use a high-gain operational amplifier to self-bias the phototransistor and thereby improve its response time. The transistor helps the op amp make the conversion by contributing to feedback; the op amp supplies current to keep the transistor at a more optimum operating point.

The circuit amplifies very low-level modulated light signals. The amplifier, compensated for a gain of 1,000, is saturated by a light level of 100 nanowatts from a 900-nanometer source. Output rise time is well under 1 microsecond at this level.

Selection of component values for other applications begins with determination of the emitter quiescent current to be provided by V_1 and R_1. The best choice generally is a current near the maximum point on the transistor's beta-vs-collector-current curve. This value will minimize changes in circuit gain with changes in signal amplitude. V_2 may have to be reduced to avoid exceeding the power dissipation rating.

Emitter current equals $V_1/R_1 - E_o/R_2$ when the amplifier's output voltage is sufficient to supply base current through R_3 and R_4. However, the quiescent current essentially is $|V_1/R_1|$ since high conversion gains $|V_1/R_1| >> |E_o/R_2|$.

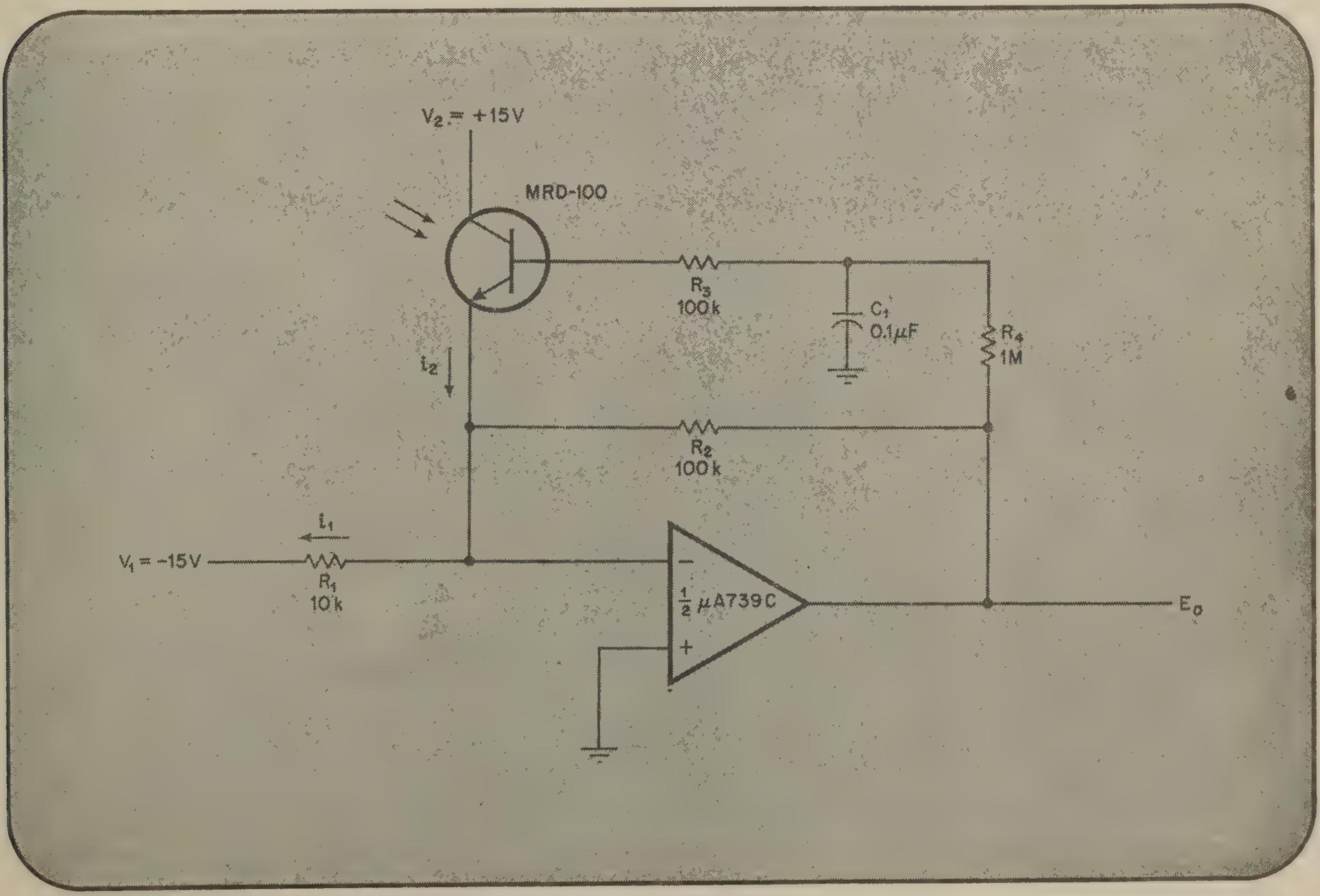
The filter formed by capacitor C_1, R_3 and R_4 is designed to cut off below the lowest desired frequency component of the input optical signal. R_3 must be large enough not to divert any appreciable fraction of the photo-generated collector-to-base current. Together, $R_3 + R_4$ should supply adequate base current when the amplifier output is 2 or 3 volts above ground.

The circuit's voltage gain within the signal band is:

$$\Delta e_o = -\Delta i_2 R_2 = -K \Delta \phi R_3$$

where K is the transistor's conversion factor at the selected bias point, in mA/(mW/cm^2) and $\Delta \phi$ is the change in illumination in mW/cm^2 or in lumens.

Photo-optical bootstrap. A constant flow of emitter current during quiescent operation makes the phototransistor ready to respond to rapid changes in intensity of low-level optical signals. Then signal current generated by the phototransistor is converted to voltage by the operational amplifier. The op amp also biases the transistor.



Nonlinear logic detects voltage tolerance levels

by R.N. Basu and A. Dvorak
Bell-Northern Research, Ottawa, Canada

A nonlinear NAND gate in a voltage detector circuit won't switch low until the gate inputs rise well above a conventional NAND's logical 1 level. Thanks to this property, the circuit can detect, with a single gate, whether a signal or supply voltage is within a nominal range, or is too high or low.

The other components establish the nominal range of the dc input voltage V_{in}, which must be done in any detector. So the circuit is quite simple and inexpensive compared with other high-low detectors. High and low levels usually are detected by two transistor circuits containing zener references, by a differential amplifier, or by other circuits that are difficult to make sensitive with good temperature stability. They are costly by comparison, particularly when voltages must be detected at a number of points.

The voltage range can be changed to suit the application as long as two conditions are met:

$$V_L = V_{ref}, \text{ at } V_{in} = V_{min}$$
$$V_H = V_c, \text{ at } V_{in} = V_{max}$$

where V_L and V_H are the minus and plus tolerances chosen with potentiometer R_1; V_{ref} is the reference voltage established by varistors R_2 and R_3; and V_c is the threshold at which a high-input V_g makes the gate output V_o go low.

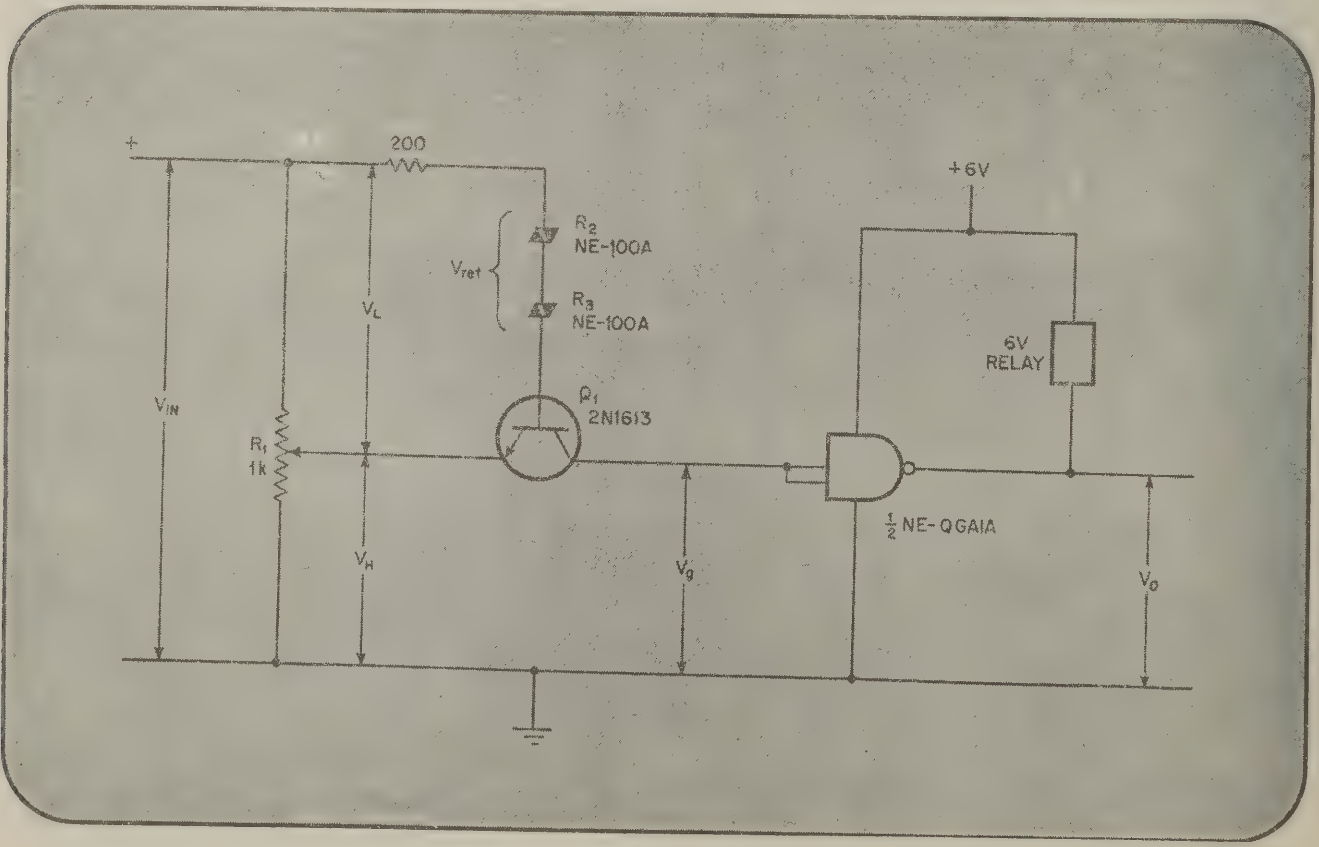
The components and potentiometer setting of this circuit were selected so that $V_{in} = 4$ V ± 1 V.

In this case, transistor Q_1 will be biased on by V_L as long as V_{in} is not lower than 3 V. When V_{in} is between 3 and 5 V, the gate output is high, detecting a normal condition. If V_{in} rises above 5 V, the increase in V_H will cause V_g to exceed the gate's threshold and the gate output will go low. It will also go low if V_{in} drops below 3 V because Q_1 will be cut off.

V_{in} can be a filtered and rectified sample of an ac signal. The choice depends on the actual voltage and stability required, and cost. The number of varistors can be changed to meet particular reference voltage and precision requirements. Or the varistors can be replaced by a zener diode. However, the varistors are less costly.

Since the circuit is digital, the outputs of two or more detectors can serve to perform control logic functions. The example shows how the output could operate a sensitive relay.

Bilevel detector. Nonlinear NAND gate generates a low output if V_{in} is too high or too low, and a high output if V_{in} is within tolerance. Q_1 conducts while V_L exceeds the reference voltage through D_1 and D_2, but if V_H and V_g become too high, V_o goes low. When V_L drops below V_{ref}, Q_1 opens and also causes V_o to go low.



Op amp splits supply for other op amps

Robert D. Pierce
Gaithersburg, Md.

When operational amplifiers require a split power supply, and only one voltage is available, an extra op amp can serve as a supply divider. The unit can provide positive and negative voltages, and balance them with feedback control.

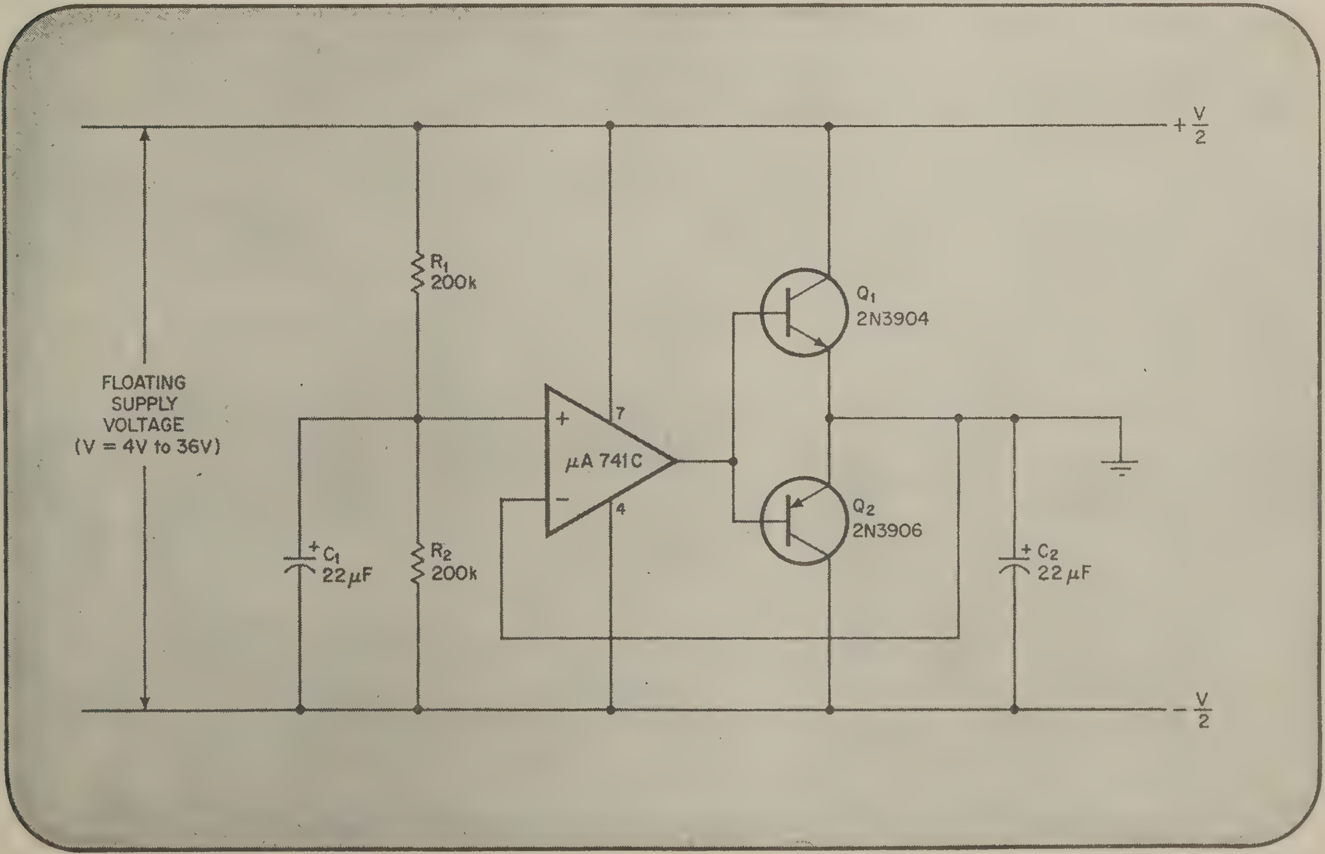
Resistors R_1 and R_2 divide the voltage on the floating input. The control circuit essentially is a low output impedance follower with complementary current boosters in the feedback loop. Current flows into or out of ground when the outputs are unbalanced; the differences in positive and negative feedback drive the outputs back toward balance.

Good balance is maintained because small output variations result from a relatively large current flow. For example, if the input is 30 volts the outputs would be only 2 or 3 millivolts apart in absolute magnitude for a current change of 10 mA. If no current is required from ground to power this circuit, total flow is only 2.5 mA.

Transistors Q_1 and Q_2 must dissipate an amount equal to ½ IV, where V is the input voltage and I sourcing and sinking current. These transistors can safely dissipate 150 milliwatts. Capacitor C_1 reduces noise and prevents possible oscillations, while C_2 helps absorb current transients.

Voltage regulation is about as good as the parent supply's since the outputs are ±½V. Voltage range that can be handled depends on the op amp type. Because the unit supplies itself in this circuit, ±½V cannot exceed the device's specification. The maximum for the μA741C is ±18 V allowing V to be as high as 36 V. This unit was selected because it is internally compensated, and has overload protection.

Two supplies from one. While R_1 and R_2 divide the input supply voltage, feedback currents force the operational amplifier to keep the output voltages equal and opposite. Transistors handle most of the power dissipated and also improve balance control by acting as current boosters in the feedback loop.



Voltage changes frequency of multivibrator by 10,000:1

by Matthew J. Fisher and John Byrne,
Drexel University, Philadelphia, Pa.

A simple addition to conventional astable multivibrators can provide significant improvements in frequency range and duty cycle. Moreover the astable circuit is easily converted to monostable operation while retaining the operational features of the former.

The basic circuit is quite simple. The control voltage, V_c, determines the time it takes to charge the capacitors, so a broad range of frequencies can be selected. The more complex circuit is self-starting; it can be used as a free-running multivibrator and has extra components to improve output pulse shape.

Operating frequency varies between 1 hertz and 12 kilohertz with the components shown, at control voltages between V_{cc} and 2 volts. Upper frequency limit of the basic design depends on the maximum value of the current source and the size of the timing capacitors. Leakage currents determine the lowest practical frequency (theoretically, the minimum is 0 Hz because $V_c = V_{cc}$ would make the charging time infinite).

Transistors Q_1 and Q_2 in the basic astable circuit are the primary switching elements. Q_3 and R_1 form, with the control voltage, a constant-current source that charges timing capacitor C_1. Q_4 and R_2 later perform the same service for C_2.

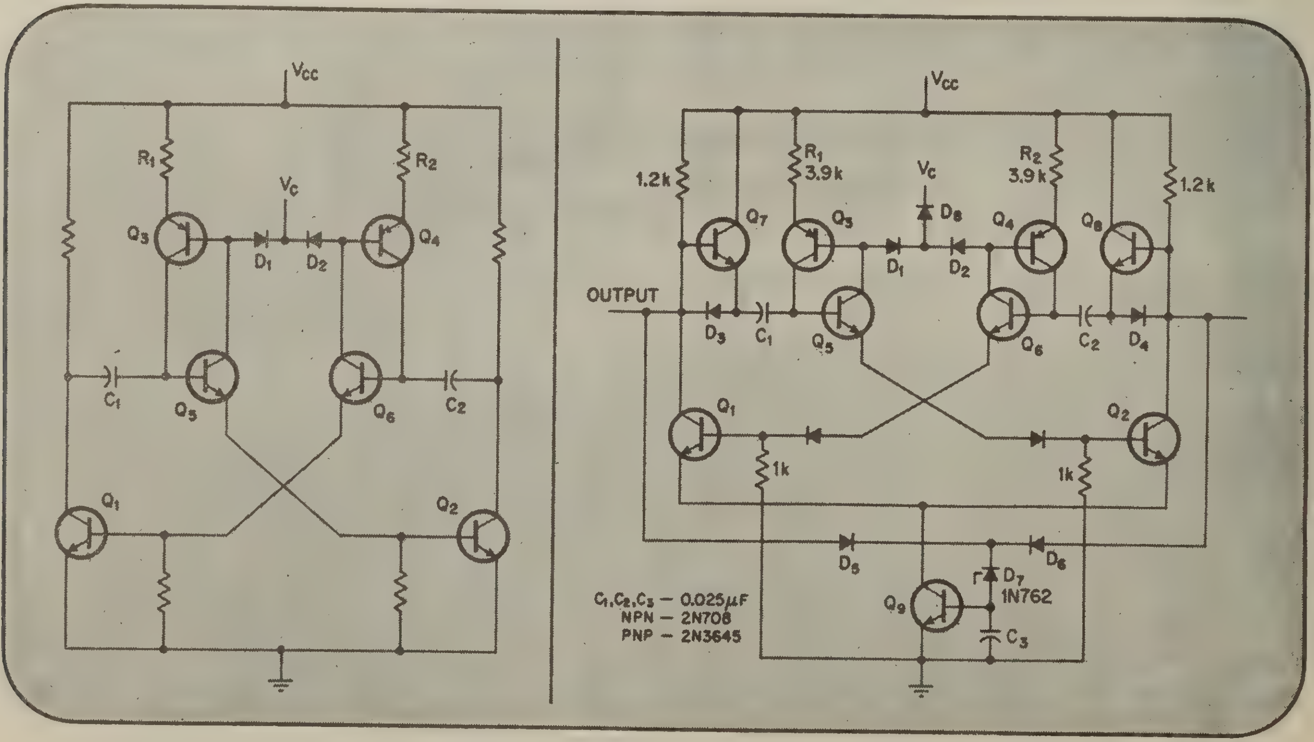
The frequency control circuit consists of these sources, plus Q_5 and D_1 or Q_6 and D_2. The diodes permit the voltage at the base of Q_3 or Q_4 to be less than V_c without affecting side-to-side switching.

A half-cycle begins when Q_1 saturates. Voltage at Q_5's base is forced negative to approximately $-V_{cc}$. Now Q_5 and Q_2 are driven into cutoff by the negative voltage and the constant-current source can charge C_1. Transistor Q_5 starts to conduct when the voltage on C_1 rises slightly above ground. As Q_5 conducts, it forms a forward-biased pnpn switch with Q_3. Then resistor R_1 can bias Q_2 into saturation, reversing the state of the circuit and starting the second half-cycle.

To make the edges of the output pulses more vertical, Q_7, Q_8, D_3 and D_4 may be added. Self-starting operation is assured by Q_9, D_5, D_6, and D_7. Maximum output voltage is clamped by the zener reference voltage. Open-circuit voltage at the bases of Q_1 and Q_2 must be kept below the zener voltage by the bias resistors.

Collector-base voltages may reach $2V_{cc}$ in the control transistors in the basic circuit. Types that can withstand $V_c + V_{cc}$ should be selected for the complex circuit. Parasitic capacitance problems will be diminished if fast switching transistors with small collector-to-base capacitance are used. Also, output will be unbalanced by variations in component values. Unless compensation is added, imbalance becomes accentuated at the lower frequencies.

Dial a frequency. Timing capacitors C_1 and C_2 don't control frequency directly. Control voltage determines charging time and can vary the multivibrator period. Q_1 starts C_1's charging by cutting off Q_5 and Q_2 and turning on constant-current source R_1 and Q_3. The charge causes Q_2 to go into saturation and start C_2 charging.



Supply tester outdoes scope as ac noise meter

by Louis F. Caso and Joseph Fazio
Bethpage, N. Y.

A voltmeter can be used to measure the absolute peak-to-peak amplitude of low-level ac noise—regardless of waveshape—with the help of operational amplifiers. What's more, the combination will do the job better and faster than an oscilloscope, reducing measuring errors to ±1%, compared with the visual test norm of about ±3%.

The circuit is used in automatic production testing of dc power supplies with tight specifications. It detects output ripple and inductive-switching spikes regardless of the positive-negative asymmetry of the noise waveform. The output is a true pk-pk total because the amplifiers bring portions of the waveform that fall below the threshold of the detector diodes back above threshold. Output ripple often can fall below conventional detector thresholds.

Amplifier A_1 and its diode–capacitor network detect and filter the positive peak levels (V_1) of the ac noise input E_{in}. A_2 inverts the waveform so A_3 can detect the negative peaks and deliver a positive voltage (V_2). V_1 and V_2 then are summed by A_4. The total V_T is negative but is the same magnitude as the pk-pk noise. Input-output relationship is linear from near zero to about 3 V. Input capacitor C_1 restricts E_{in} to just the ac noise component riding on the dc output of the supply under test.

When V_1 drops below the diode's threshold voltage, V_1, D_1 won't conduct; the high feedback resistance then boosts A_1's gain above unity. When V_1 goes above threshold, D_1 conducts. This allows C_2 to charge to the input signal and decreases the feedback resistance so that A_1's gain again is unity.

A_2 is a unity-gain inverting amplifier, so A_2 and A_3 in combination work the same on the negative portion of E_{in} as did A_1 on the positive. D_2 performs identically to D_1.

According to the superposition theorem, the voltage at the junction of R_1 and R_2 is:

$$V_j = (R_1V_1 + R_2V_2)/(R_1 + R_2)$$

It is desirable to make $R_1 = R_2$ and use R_3 for calibration. This makes $V_j = \frac{1}{2}(V_1 + V_2)$.

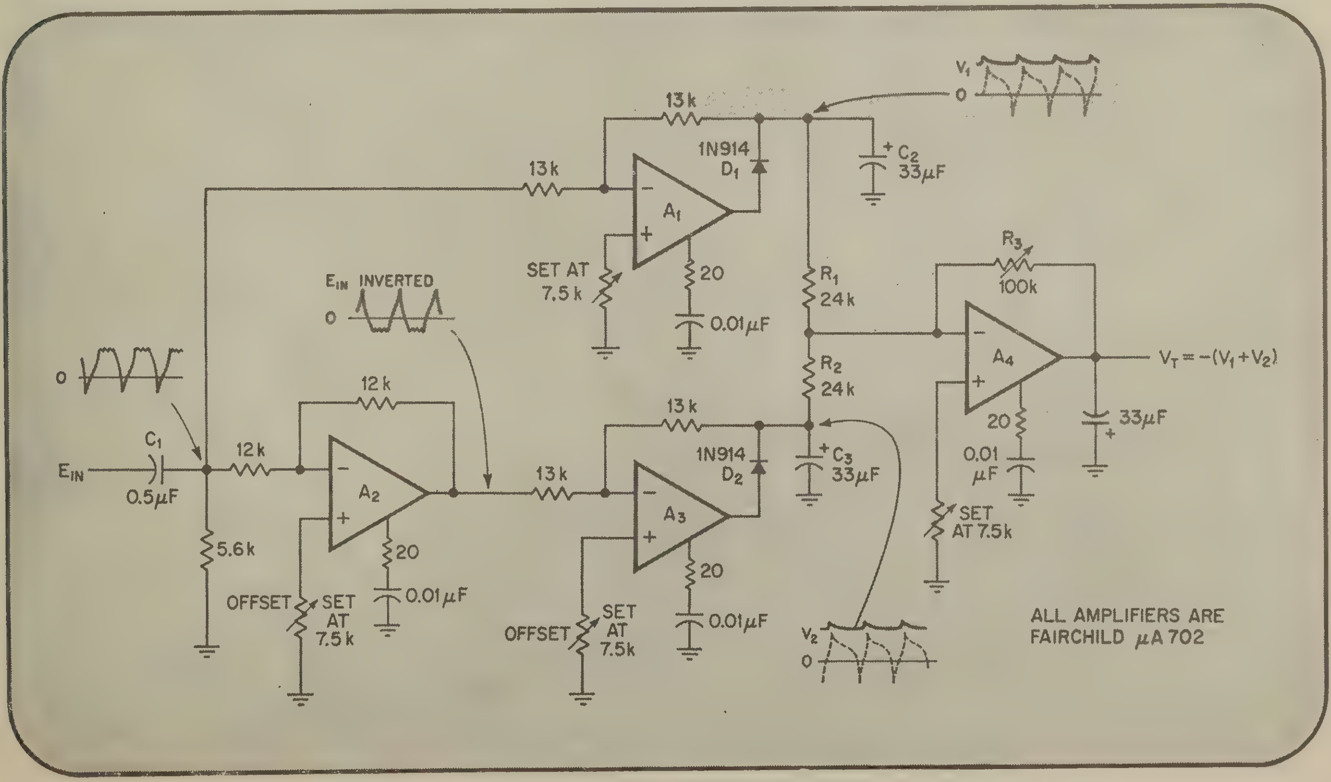
However, when this voltage is summed by A_4, the dc output voltage is:

$$V_T = -R_3\ (V_1/R_1 + V_2/R_2)$$

Therefore, if $R_1 = R_2$ all that is needed to make V_T equal $-(V_1 + V_2)$ is to set the feedback resistor R_3 equal to $R_1 + R_2$ or 48 kilohms.

V_T is negative because A_4 inverts. An output inverter similar to A_2 will make it positive, but the inversion is not needed by most test instruments.

Ripplemeter. Magnitude of asymmetrical noise waveform is detected by converting the positive and negative peak values to two voltages which are then summed. Amplifier A_1 and its diode-capacitor network find the peak positive value of the signal level; A_3 finds the negative peak. A_4 sums V_1 and V_2.



Counter shifts signal phase only one way

by Peter J. Kindlmann
Yale University, New Haven, Conn.

Twisted-ring counters do a better job of generating phase-shifted waveforms than flip-flops connected in a more straightforward way. The phase shifts on the counter outputs aren't ambiguous, and the counter takes fewer logic devices.

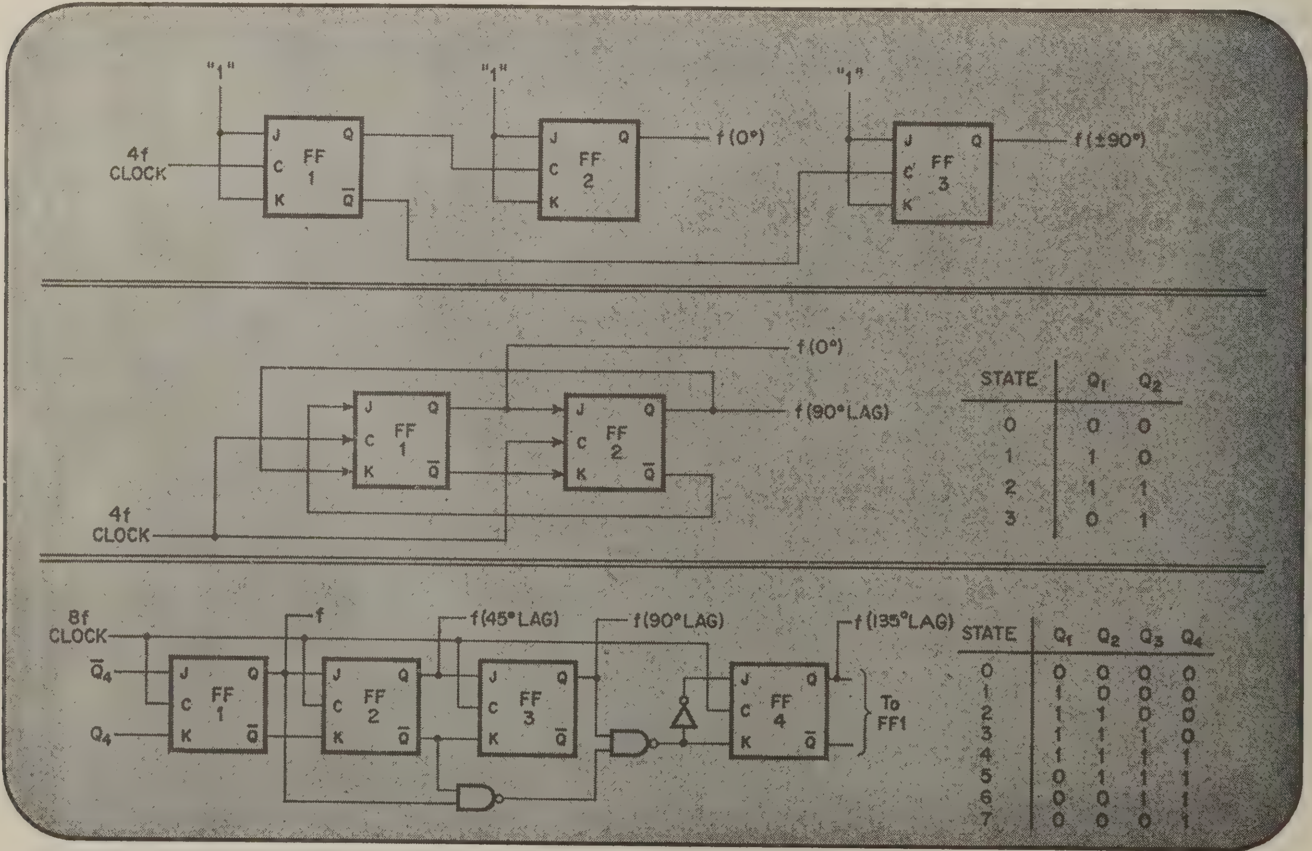
An assembly of three flip-flops, like the first circuit below, has been used in the past to generate waveform pairs with a 90° phase difference. But the sign of the phase difference is not well defined because the flip-flops operate in the toggle mode. Their phase ambiguity is ±180°.

Connecting just two J-K flip-flops as a twisted ring counter produces the state sequence shown in the truth table. The Q output of flip-flop 2 always lags the output of flip-flop 1 by 90° no matter which state initiates the sequence when the clock pulse is applied.

A variety of other phase shifts can be obtained by adding stages to the twisted-ring counter, as the four-stage version illustrates. The flip-flop states may be arbitrary when power is first applied. The fourth stage and its input gating insures initiation of the correct state sequence. The state steering of flip-flops, as illustrated by the truth tables, provides outputs with successive phase shifts. Each is shifted the same amount.

The two-stage counter is sufficient for most applications such as motor drive, phase-sensitive detectors and single-sideband modulators. Some applications require filtering of the digital outputs. Filtering is quite easy since the outputs are symmetrical square waves and there is a 3:1 frequency ratio between the fundamental and lowest harmonics.

Lag or lead? A system using the old-style phase shifter made with toggled flip-flops cannot tell which output leads and which lags. But the sequence through the twisted-ring counters guarantees that each of the outputs lags the first by a fixed amount even when the starting states are arbitrary.



STATE	Q_1	Q_2
0	0	0
1	1	0
2	1	1
3	0	1

STATE	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Series limiter tracks signal, finds symmetry

By Roland J. Turner,
RCA Corp. Missile Surface Radar division, Morristown, N.J.

Multichannel limiting with a single series limiter is a lot less expensive than having a shunt limiter in each channel. But symmetry suffers when the reference dc level is fixed and the signal level isn't. However, a series cutoff limiter preserves symmetry via a unique feed-forward design that makes V_{ref} track V_{in} during class A operation. Interference inputs block themselves by driving one output diode to cutoff.

The series high-voltage tracking, symmetrical cutoff limiter shown limits 10 video channels simultaneously. It costs about one-tenth as much as the shunt limiter it replaces and is much more efficient. When activated by a high-level interference signal, the limiter acts as a current switch. Since no current is drawn from the source driver, that circuit can be an inexpensive, low-current device, too.

During quiescent operation, input and output diodes D_1 and D_2 are biased in their class A region. They draw current equally from their current source because the dc voltage levels at their cathodes are matched. The currents are 11 milliamperes.

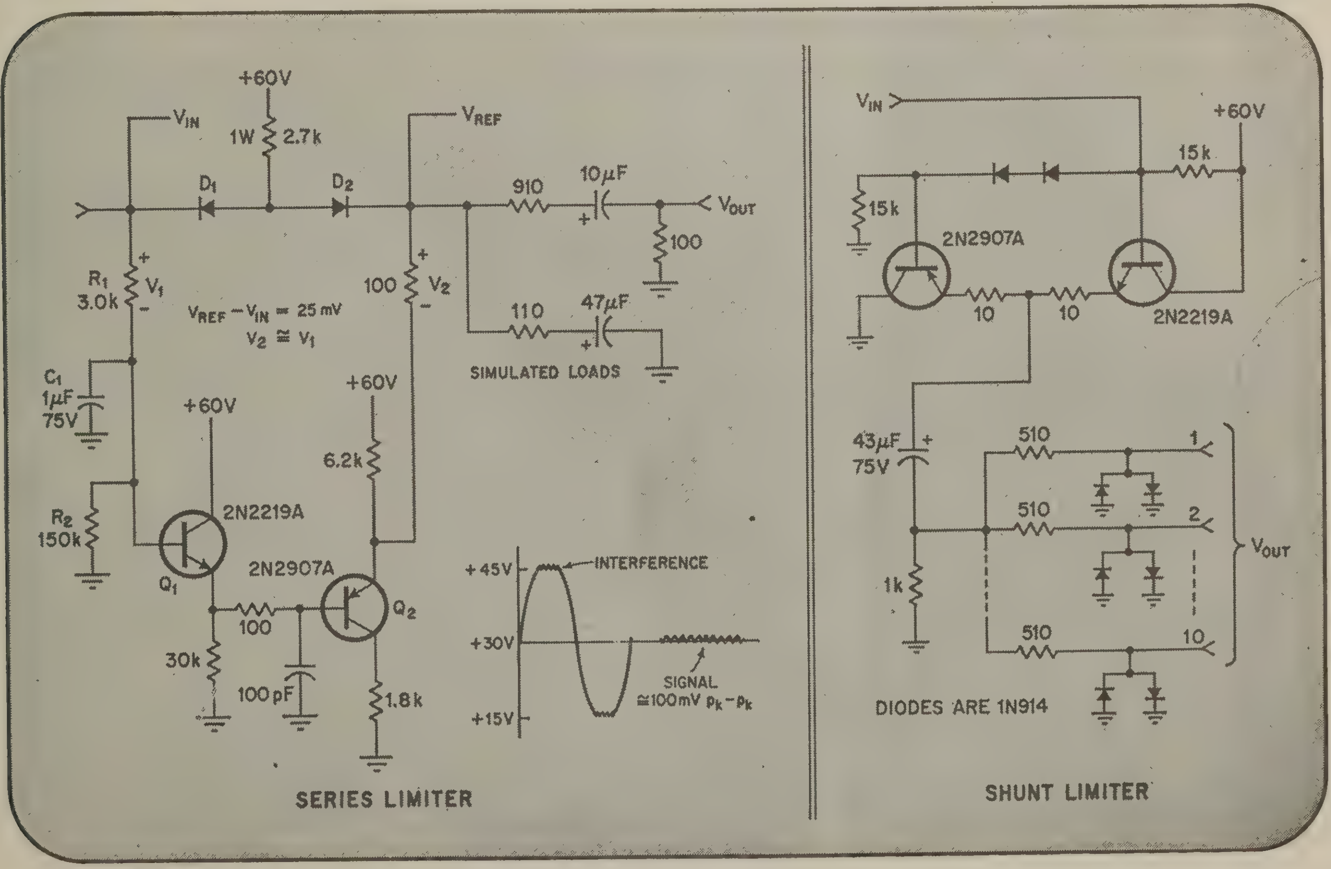
The match is made by extracting the input dc level with low-pass filter R_1C_1 and passing this level through transistors Q_1 and Q_2. The voltage drop, V_2, caused by the quiescent current drop, is compensated with R_2. This resistor establishes an opposing voltage drop, V_1. The quiescent voltage differential across the two diodes $(V_{ref} - V_{in}) = 25$ millivolts. Since Q_1 and Q_2 are complementary, their emitter-base voltage drops cancel and the output tracks the input over a wide temperature range.

Any interference signal above 400 mV drives the series limiting diode to cutoff and no interference can appear across the output.

In class A performance tests, composite signals up to 140 mV peak-to-peak passed through the limiter with low harmonic and intermodulation distortion. A 140 mV, 10-kilohertz signal produced harmonic distortion products less than —44 decibels. Two 70 mV input signals, one at 12 kHz, the other at 15 kHz, produced intermodulation distortion products less than —46 dB.

The main benefit of tying V_{ref} to the average signal level is that a large coupling capacitor is no longer required. This capacitor alone costs $28.50 in the shunt limiter, while the total parts cost of the series limiter is $3.

Tracking unlimited. Reference voltage of series limiter tracks the average input level. This allows low-level signals to pass with little distortion, but diodes cut off the higher interference levels. A shunt limiter, however, must block high voltage with a large, expensive high-quality capacitor to maintain a ground reference.



OP amps delay and shape data signals

by Barry M. Kaufman
Vega Electronics, Santa Clara, Calif.

Symmetrical operation, continuously adjustable delay times, and low cost are features of a delay equalizer for digital communications systems. It has been used in a high-speed modem to achieve coincidence among data signals transmitted over circuits that have different propagation delays. Signals arriving early are delayed as needed by changing the potentiometer setting.

Amplifier A_1 is a buffer that shapes the input pulses. Voltage divider R_1 and R_2 prevents the input from exceeding the amplifier's common-mode range. If the input pulses have fast rise and fall times and if they swing between the positive and negative potentials of the power supplies, A_1 isn't needed—A_2 alone will delay such pulses and keep them square.

A_2's output follows the negative-going and positive-going transitions of A_1's output after a delay of about 0.3 R_4C_1. If the output of A_1 is at the positive bus level, the noninverting input of A_2 rests at 5.7 volts and C_1 is charged. Or, when A_2's input is negative, the rest level is −5.7 volts, and C_1 is discharged. The two rest levels are set by the drops across the diode combinations of D_1 and D_2 and D_3 and D_4, respectively.

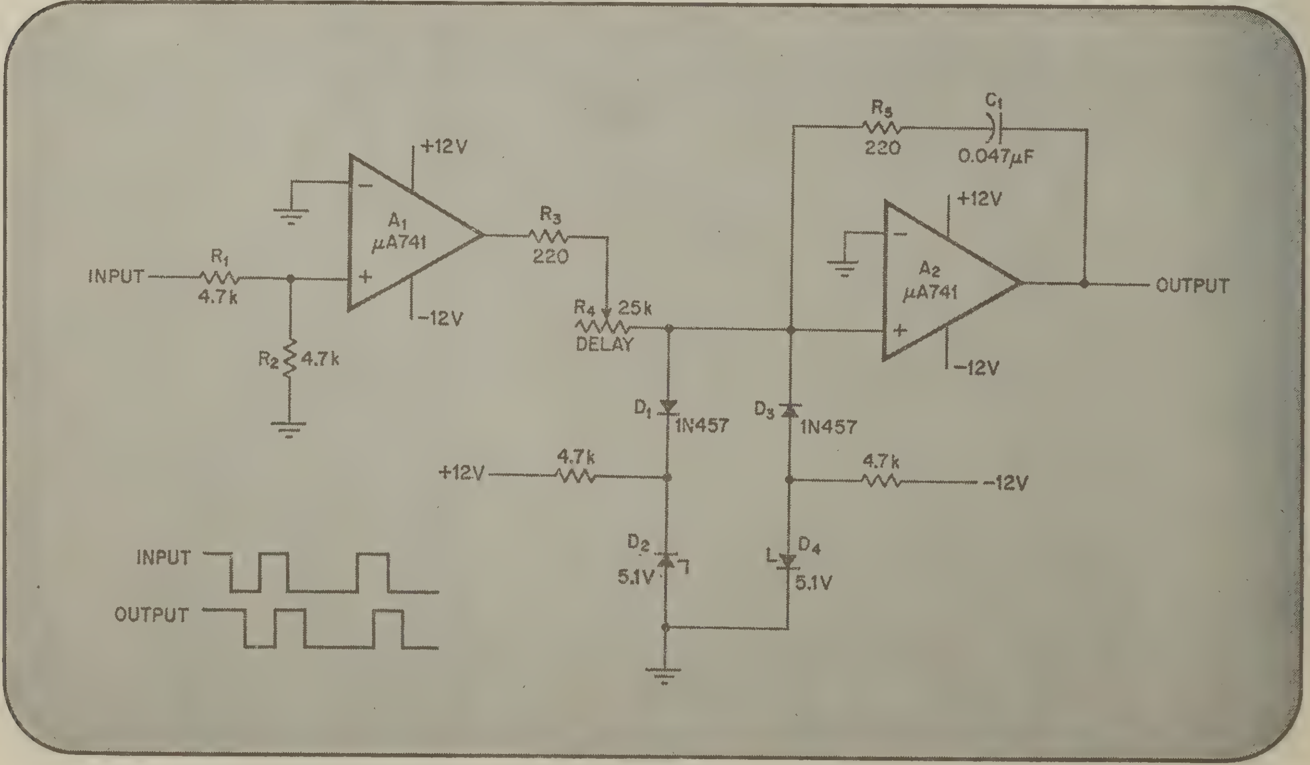
A_1's output swings from negative to positive, current through R_3, R_4, and R_5 begins charging C_1 toward the positive level. After the RC time, the voltage on A_2's input rises through zero and the output goes positive abruptly. Positive feedback coupled through C_1 and R_5 drives the input hard to the positive rest state. A swing from positive to negative reverses the action and output polarity with the same delay.

Because the delay times are equal, there is no bias distortion of the signal. The equality of the delays is assured by matching the zener voltages of D_2 and D_4 (the drop across D_1 or D_3 when they are conducting is a semiconductor constant, 0.6 volt).

Reset time is very short compared with a data bit length. Time delay is not a function of signal pulse width or pulse duty cycle, since C_1 is rapidly charged or discharged through a relatively low impedance. Delays up to 80% of the shortest bit time are obtained. With the RC values shown, they last from 50 to 400 microseconds; if C_1 is larger they can range up to tens of milliseconds. R_3 and R_5 mainly limit surge currents and have little effect on timing.

The circuit operates at a data rate of 2,000 bits per second in the modem application. An amplifier such as the μA 748 may be substituted for the internally compensated μA 741 if the 741's slew rate is too slow for higher-frequency applications.

Delay equalizer. Potentiometer R_4 adjusts signal delays in communications circuit. It changes the time required for C_1 to charge or discharge by varying the current flow around A_2. The RC time constant determines when feedback into A_2 will drive the output to follow the input. Diode drops stabilize voltages and delay times.



Amplifiers let voltmeter measure op amp noise

By Richard C. Gerdes,
Optical Electronics Inc., Tucson, Ariz.

Special instruments aren't needed to measure the noise generated by an operational amplifier. Peak-to-peak, root-mean-square, and even spectral-density noise characteristics can be measured with an ordinary panel meter or digital voltmeter.

The test circuit makes the amplifier under test (AUT) generate highly amplified noise peaks. These are detected and then simply scaled down to find the noise values. Measuring errors are less than 1%, small enough to test op amps for critical applications such as low-level jobs, instrumentation, and video circuits.

One part of the noise meter is a test board with ground inputs for the amplifier under test, a feedback resistor chosen to give the amplifier a gain of 100, and an isolation network to minimize power supply noise, which could, if large enough, cause inaccuracy.

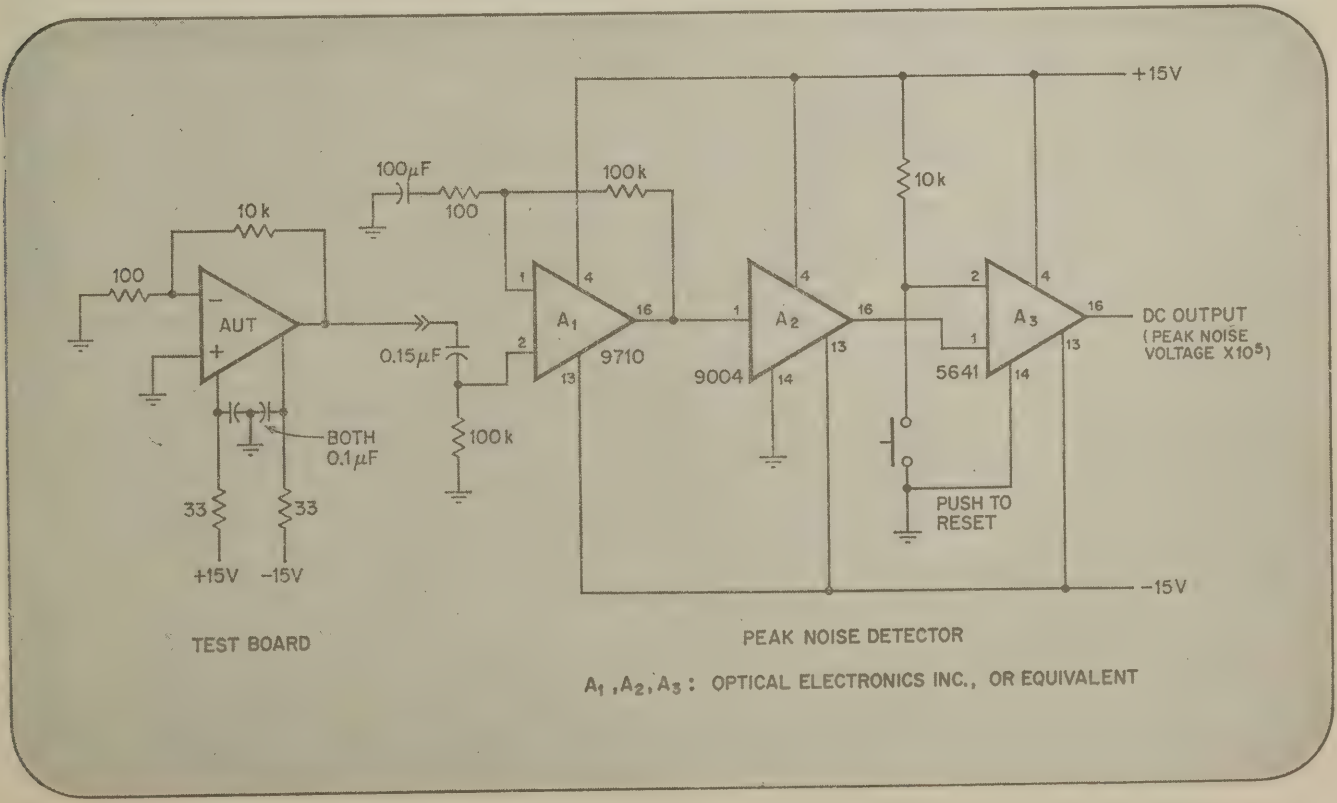
The test board plugs into a detector circuit with a gain of 1,000, (preamplifier A_1). A_1 is an operational amplifier with field effect transistor inputs. Noise bandwidth is 10 hertz to 10 kilohertz.

A_1 drives A_2, an absolute-value circuit that detects or rectifies the ac noise voltage to a dc voltage with positive polarity. The unipolar noise signal drives A_3, a module that senses and holds the peak noise value.

Together, A_2 and A_3 ensure that the largest noise peak is captured and presented to a voltmeter connected to the dc output, regardless of that noise peak's polarity. After the amplifier under test is plugged in and the power supplies turned on, the reset switch is closed for 10 seconds. This sampling period permits capture of low-frequency noise transients.

Since the total gain in the test board and in the preamplifier is 100,000, a 1-volt reading on the voltmeter represents a peak noise voltage of 10 microvolts, 20-microvolts peak-to-peak noise or 3.3-μV rms noise. If the amplifier under test has a gain-bandwidth product of at least 1 megahertz, it is fairly safe to assume that the spectral noise density in μV/Hz is the meter reading in millivolts divided by 30.

Noise detector. Noise generated in the amplifier under test is amplified by 100 on the test board and by 1,000 in preamplifier A_1. Amplifier A_2 detects or rectifies the noise peaks as a positive voltage that is stored in A_3. The output of A_3 is a smooth, dc voltage 100,000 times the peak noise level; it is easily measured and scaled.



FET pair bridges meter impedance gap

By Jack Theodore,
Tri-Electronics, Hammond, Ind.

Operating as a differential pair, two monolithic junction field effect transistors can increase the sensitivity of a high-resistance bridge's galvanometer null detector. Accuracy of zero-balancing thus is increased. The small, inexpensive FET circuit can be battery powered, and fits easily into bench or portable instruments. In fact, with carefully selected range resistors, the detector can serve as a good general-purpose voltmeter.

An unaided galvanometer will lose sensitivity as the bridge resistance values are increased. But with the J-FETs the detector's terminal resistance can be very high. For best sensitivity, the terminal resistance should equal the series-parallel resistance of the bridge arms (a galvanometer usually has a low, fixed resistance).

Also, because both transistors are on the same substrate, differential drifts due to temperature changes are limited to the low-microvolt range.

The circuit is built around a galvanometer with a coil resistance of about 350 ohms and a current sensitivity of 0.15 microampere per scale division. There are 30 scale divisions on each side of the zero point.

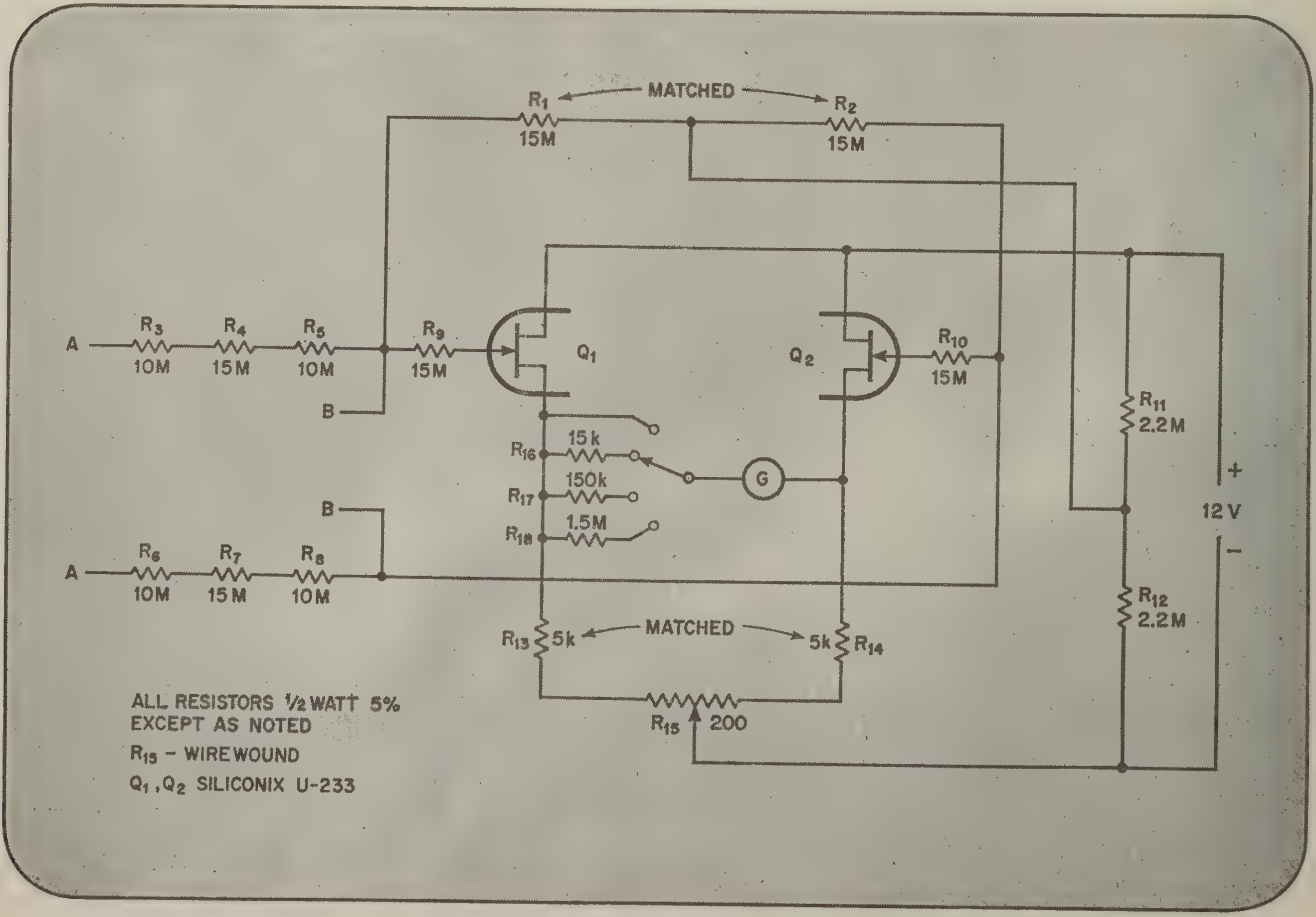
Input resistance at terminals A-A is established at 100 megohms by voltage-divider resistors R_1, R_2 and R_3 through R_8. Only 30% of the input voltage appears across the gate-load resistors, R_9 and R_{10}. The gates are biased from the junction of voltage divider R_{11} and R_{12}. Source resistors R_{13} and R_{14} drive the galvanometer. Small differences in the currents through the two sides are balanced out via potentiometer R_{15}.

Sensitivities ranging from 1 volt per scale division to 1 millivolt per division can be selected with the switch. Zero adjustment is made on the most sensitive range after the detector is connected to the de-energized bridge circuit.

The FET detector is more sensitive than the galvanometer alone at bridge values above 10 kilohms. The unaided meter's sensitivity is better at lower bridge resistances.

Sensitivity may be improved by using terminals B-B, which reduce input resistance. But care must be taken that the transistors' gate breakdown voltage is not exceeded.

FET null detector. Transistors Q_1 and Q_2 improve the galvanometer's sensitivity when nulling a bridge with high-resistance values. Input resistance is raised to 100 megohms by resistors R_1 through R_8. The transistors operate as a differential pair, biased with a dc supply. Switch ranges are 1 volt to 1 millivolt per meter division.



1-volt cell powers mini audio amplifier

By Don G. Jackson,
Resalab Inc., Garland, Texas

An audio amplifier designed specifically for micropower applications features automatic gain control, a large dynamic range, and high efficiency from a low-voltage supply.

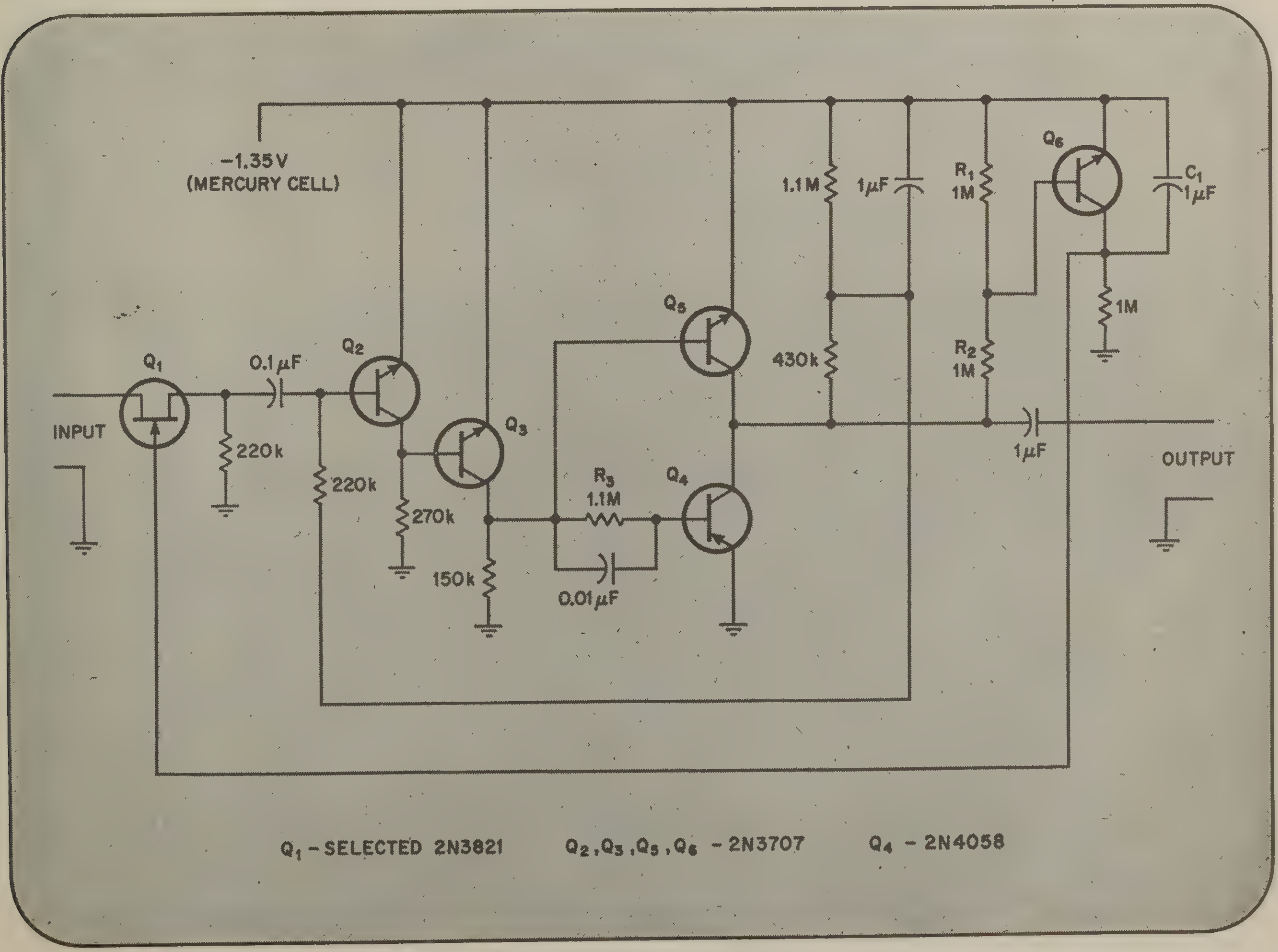
Maximum output level is about 1 volt peak-to-peak across a 5-kilohm load. Typical gain is 65 decibels. The amplifier draws only 50 microamperes of current from a 1.35-V mercury cell and has an overall efficiency of about 40%. Tradeoffs among current drain, efficiency, output impedance, and crossover distortion may be made by changing component values.

Automatic gain control is accomplished by detecting the output signal and feeding back the resulting dc signal to the gate of the series field effect transistor, Q_1. This varies the channel resistance of the junction field effect transistor. Transistor Q_6 is the AGC detector. Although the FET type is not critical, it should be selected for a $V_{GS(off)}$ of 1 V or less since the output signal is limited to 1 V pk-pk. Output voltage in the AGC range depends on resistors R_1 and R_2; both are 1 megohm for 1 V pk-pk.

Transistors Q_2 through Q_5 form a complementary output, current-driven amplifier. Output level is limited by the $V_{CE(sat)}$ of Q_4 and Q_5. Bias is stabilized by dc feedback. Resistor R_3 and the h_{fe} of Q_4 essentially set the current drain (50 μA). Currents in the other portions of the circuit remain low because they are clamped by the feedback, base-emitter voltages, and the supply voltage.

Low-frequency response is controlled largely by bypass capacitor C_1 in the dc feedback loop. A 1-microfarad capacitor sets the 3-decibel low-frequency cutoff at about 270 hertz. The 3-dB high-frequency point is about 4.5 kilohertz. Depending mainly on the signal-source impedance, the low-frequency rolloff can exceed 6 dB per octave.

Micropower microamplifier. Powered by a 1.35-volt mercury cell, audio amplifier is basically a current-driven device with complementary outputs at Q_4 and Q_5. Gain is controlled by detecting the output with Q_6 and feeding back the dc signal to control series FET Q_1. The components shown limit the output to 1 V peak-to-peak.



Avalanching transistors speed up high-voltage pulses

By Erwin A. Jung
Argonne National Laboratory, Argonne, Ill.

Many amperes of charging current are required to develop a pulse of a couple of hundred volts across a load with a capacitance of 100 picofarads in only a few nanoseconds. It's difficult to find such pulsers even though they're often necessary in such applications as nuclear instrumentation, cathode ray tube deflection, and photomultiplier tube drivers. However, teaming up a vacuum tube and transistor provides a variable pulse of 200-400 volts with rise and fall times of 30 ns.

In the circuit, the load represents the dynode of a photomultiplier that is to be turned off during an intense illumination of its photocathode. The dynode impedance looks like about 25 kilohms paralleled by about 10 to 20 pF.

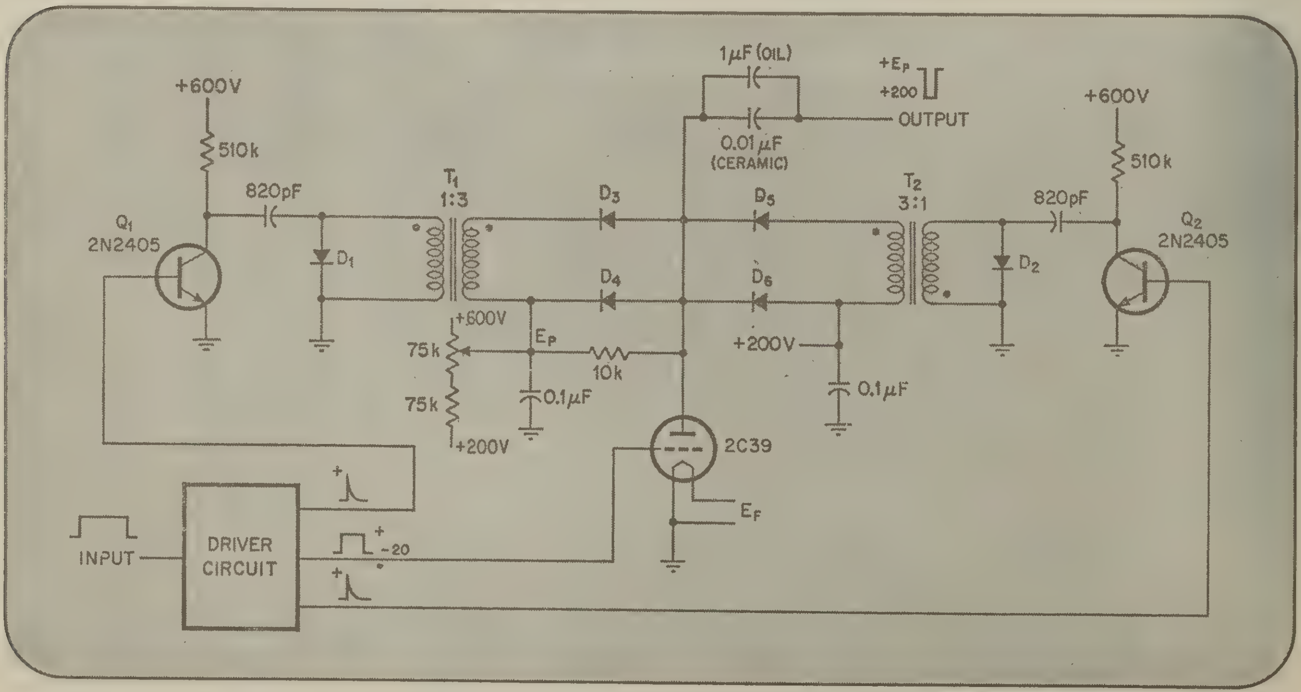
The 2C39 tube is biased at cutoff until the input blanking pulse appears; the tube then begins to conduct. The input pulse also is applied to the base of transistor Q_1, which goes into an avalanche mode. If the tube were acting alone, it would deliver an output pulse, but not fast enough. The avalanche-mode transistor helps speed things up. When the transistor avalanches, it produces a pulse that would reach 600 V at the output of step-up transformer T_1, if the plate voltage were not clamped at 200 V by diode D_6. This high-current, negative-going pulse provides fast charging of the load capacitor (through D_3, the transformer secondary, and then to ground through the filter capacitor on the E_P supply).

During the flat-top portion of the input, the tube serves to clamp the plate voltage at 200 V. The larger output coupling capacitor prevents droop in the output; the smaller assures fast rise and fall times.

At the trailing edge of the input pulse, the opposite occurs: transistor Q_2 avalanches and supplies a positive pulse at its secondary. (Note that the windings have reverse polarity.)

Diodes D_1 and D_2 prevent possible collector triggering of Q_1 and Q_2. Each of the six diodes (D_1-D_6) actually consists of six IN4148s in series. A Q_1 and Q_2 are selected for avalanche voltage greater than 250 and avalanche current greater than 20 milliamperes. Each transformer consists of 10 and 30 turns wound on ferrite toroidal cores. As shown, the circuit can handle a 2-kHz repetition rate at a 1% duty cycle.

Team work. Vacuum tube-transistor combination gives pulses of 200 to 400 volts with rise and fall times of 30 nanoseconds. Input pulse turns on the tube and drives Q_1 into avalanche mode. High current pulse charges load capacitor through T_1 secondary to provide a fast rise time. Similar action assures a fast fall time.



SCR crowbar circuit protects Impatts

By J. Nigrin
University of Alberta, Edmonton, Canada

A sudden surge of current to an Impatt diode from its bias supply can burn it out. Usually, commercially available power supplies don't react fast enough to prevent such damage. Although a resistance higher than about 10 kilohms placed in series with the bias supply would help, it also would degrade an Impatt oscillator's performance. A better solution is to use an inexpensive SCR crowbar circuit that senses the current change and shunts the current around the Impatt before any damage is done due to excessive junction heating.

In the circuit, the bias current is sensed by R_o. If it increases, speed-up capacitor C_s assures that this change quickly fires the SCR. Resistor R_2 sets the voltage and R_1 sets the current, at which the SCR turns on. Since both these resistors influence the SCR gate current, they must be adjusted by a trial method.

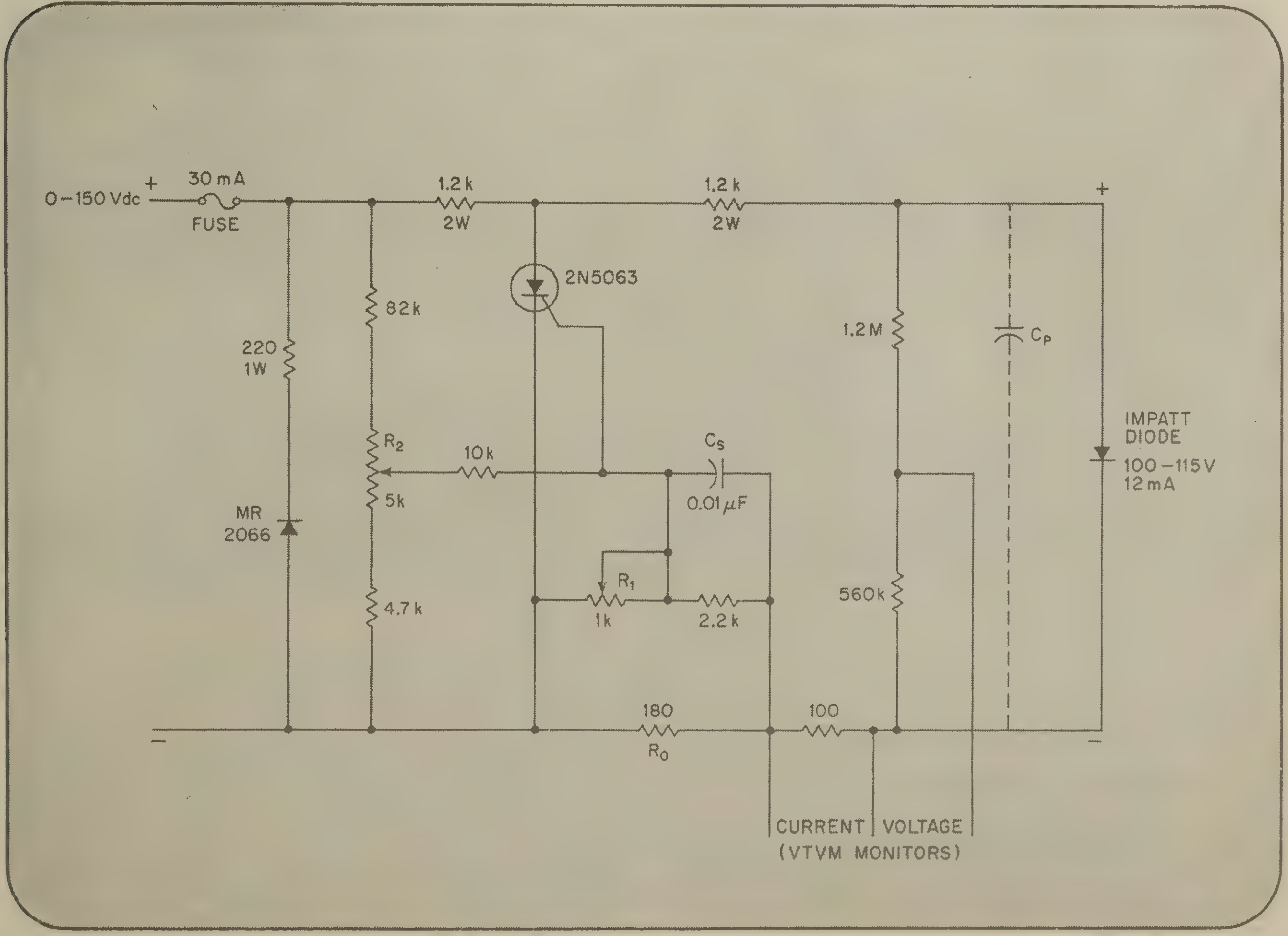
The sensing resistor R_o can be as much as a few thousand ohms since the output impedance of the bias circuit for Impatts should limit the peak current to a value a few times larger than its maximum dc value.

The circuit uses a 90-cent 2N5063, which will switch off less than 1 microsecond after the output leads have been shorted. A single 0.2-μs current pulse through the sensing resistor, with an amplitude 1.5 times larger than the switch-off current value, will switch the supply from 110 volts at 10 milliamperes to 0.5 V in less than 0.4 μs after the leading edge of the current pulse.

The MR2066 SCR shorts the crowbar input terminals if incorrect polarity is applied to the circuit. The fuse at the input is not really necessary, since the voltage drop across a fired SCR is safe enough (about 0.5 V to 1.5 V) to be handled by the Impatt. However, the fuse does offer extra protection, and requires that the user identify the trouble before replacing it.

The bias-lead capacitance, C_p, should be kept to a minimum because it will discharge directly through the diode. As such, it's best to mount the crowbar circuit inside the oscillator housing.

Blowout-proof. The Impatt diode is protected from current surges by the SCR. Resistor R_o senses any sudden change in current and couples the surge to the SCR gate through C_s. When the SCR fires, the Impatt voltage drops from about 110 V to 1 V in a fraction of a microsecond. The MR2066 diode assures correct polarity for the Impatt.



Wien bridge oscillator needs only one op amp

By P.C. Lipoma
Lockheed Electronics, Houston, Texas

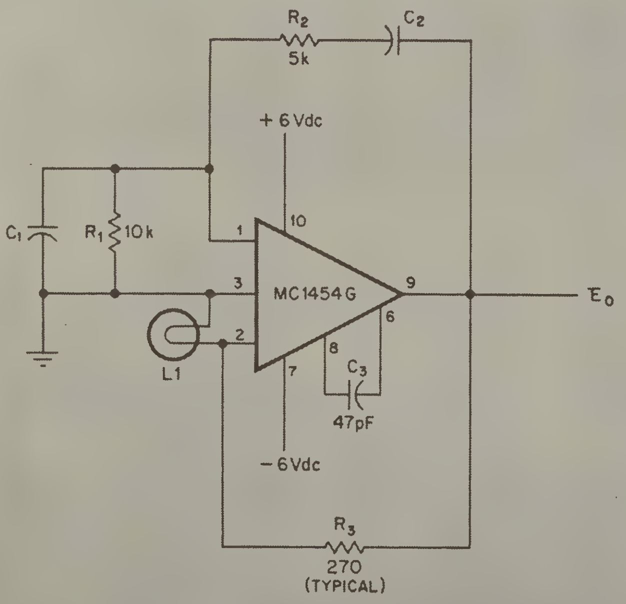
A simple Wien bridge oscillator, with good drive capability, can be built round a single operational amplifier for a cost of less than $5. The circuit consumes little power, and drives both low impedance and highly capacitive loads with low distortion.

The operational amplifier used can drive 8- and 10-ohm loads, and provides an output of from 2 to 8 volts peak-to-peak across a 10-ohm load. Its harmonic distortion is typically less than 0.5% over a frequency range of 1 hertz to 100 kilohertz.

Automatic gain control is provided by the lamp, L_1, which varies in resistance with changes in the output voltage. Resistor R_3 provides the required negative feedback, and, to a limited degree, determines the output signal amplitude. Capacitors C_1 and C_2 form the reactive portion of the positive feedback loop, and are set equal in value. Resistor R_1 is selected so that it's equal in value to the input impedance of the amplifier, while R_2 is half that value (R_1 shunted by the amplifier input impedance). Since both the series and the parallel capacitors and resistors in the positive feedback loop are equal, the frequency of oscillation is simply $1/2\pi\ R_2C_1$. High-frequency compensation is provided by capacitor C_3.

To turn this circuit into a signal generator, the only addition necessary is a switch section, to alter the values of C_1 and C_2.

Compact. The single-stage Wien bridge oscillator delivers stable output frequencies from 1 Hz to 100 kHz across loads as small as 8 ohms. The lamp, L_1, provides automatic gain control by changing its resistance as the output signal amplitude varies. The chart details the values of C_1 and C_2 required for circuit oscillation at specific frequencies.



FREQUENCY	C1, C2
1 Hz	33μF
100 Hz	0.33μF
500 Hz	0.065μF
1 kHz	0.033μF
10 kHz	3,300pF
50 kHz	650pF
100 kHz	330pF

ALL CAPACITORS ARE NON-POLARIZED

L1 = #80 (LAMPS INC. OF GARDENA, CALIFORNIA)

Sequential gate won't chop odd-length pulses

By Björn Kruse
Stockholm, Sweden

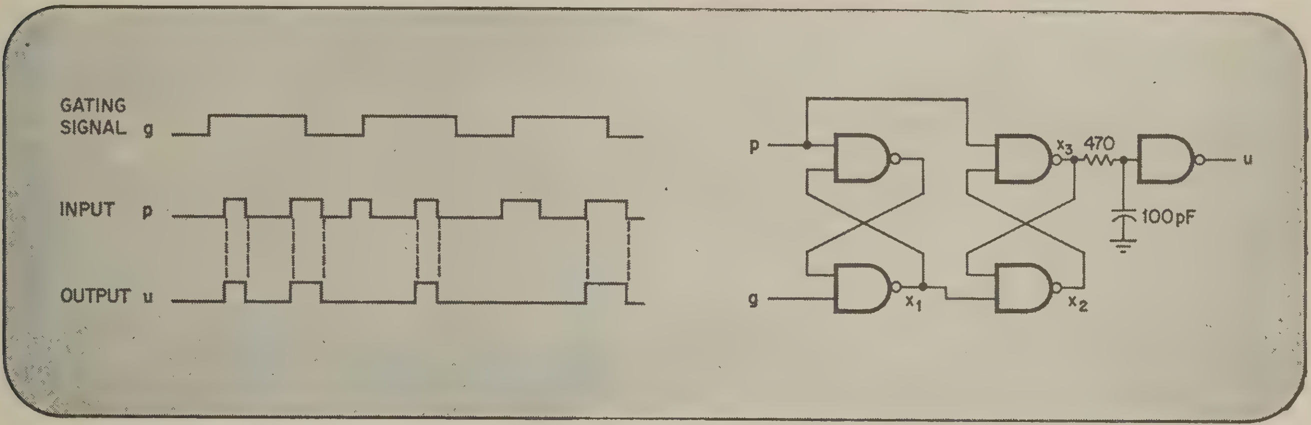
Digital systems that use varying pulse lengths require a gating circuit that won't transfer any part of a pulse unless it is enabled to transfer the whole pulse regardless of the state of the gating-control signal. The gate should turn on before a pulse arrives and not turn off until after it passes through completely.

This type of application calls for an asynchronous, sequential circuit. Fortunately, enough logic to do the job is contained in a quad NAND gate—one integrated circuit package. Connected as two flip-flops, the quad gate meets all the criteria except that it complements the data. An inverter—one-sixth of an IC—makes the output true.

The first flip-flop is reset to $X_1 = 0$ only if pulse $P = 0$ and gating control $G = 1$. With $X_1 = 0$, the second flip-flop is set to $X_2 = 1$. When X_2 is in this true state, $X_3 = 1$ also, unless both P and G are true. Then, X_3 is false, but the data appears at output U.

On the other hand, suppose $P = 1$ and G drops to logical 0. Since $X_3 = 0$ from the previous input, X_2 is still 1. Not until P drops to 0 can X_3 return to 1 and make output U drop to 0. Now the second flip-flop is reset to $X_2 = 0$, so that no pulse can appear at the output unless the first flip-flop is reset.

Door, not gate. Instead of simply gating a pulse train on and off, the circuit lets the pulses hold the gate open. The gate must be enabled before a pulse arrives to transfer a pulse; once enabled, the circuit will not be disabled until a complete pulse is transferred. If used with relatively slow circuitry, the R-C network isn't necessary.



One-shot saves power without losing time

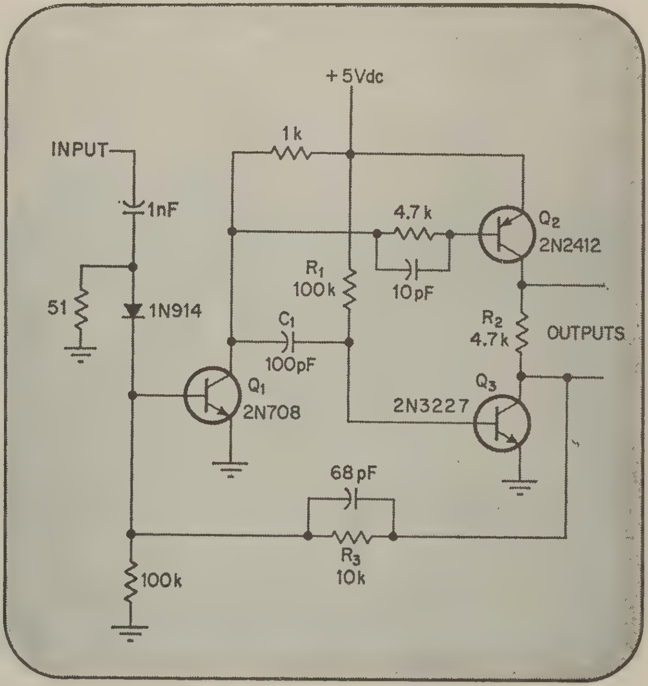
By C.H. Doeller 3rd and Aaron Mall,
Communications division, Bendix Corp., Baltimore, Md.

About 99% of the power wasted by a conventional one-shot can be conserved by using a low-current design which also offers the advantage of timing that does not depend on transistor beta. What's more, two low-impedance outputs are available, one with a positive-going and the other with a ground-going edge.

When a positive pulse is entered, transistors Q_1 and Q_2 turn on, and Q_3 is turned off through capacitor C_1. C_1 and resistor R_1 determine the time during which Q_1 is held on by Q_2 through R_2 and R_3. At the end of the timing cycle, Q_3 turns on again, turning off Q_1 and Q_2.

In the quiescent stage, Q_3 can't waste collector current because Q_2 is off. The only current that flows is that needed to keep Q_3 saturated at the desired load, reducing standby power dissipation to about 1% of the figure for a conventional one-shot.

Output pulse width is directly proportional to R_1C_1, sized here for 8.0 microseconds. Output rise times are less than 20 nanoseconds.



Very quiescent. The only current flowing in the one-shot's normal state is a low standby current through Q_3. Output pulse width is set by R_1 and C_1.

Battery discharge triggers alarm and shuts off supply

By Dean Jeutter
Drexel University, Philadelphia, Pa.

A circuit with two Schmitt triggers will activate an alarm when a battery runs down, and then will shut down a voltage regulator powered by the battery. The warning can assure swift replacement of the battery, while the shutdown prevents erratic operation of systems such as telemetry transmitters and industrial radio controls.

The two triggers are formed by transistors Q_1 — Q_2 and Q_3 — Q_4. As long as the battery is adequately charged, the second trigger circuit keeps the collector-emitter voltage of Q_5 at about 0.25 volt dc and Q_5 conducts hard. In this state the conventional voltage regulator formed by Q_6 and Q_7 can power the load.

Diodes D_1 and D_4 keep the trigger operating points nearly the same, while zener D_2 assures a stable operating voltage for Q_2 and Q_3.

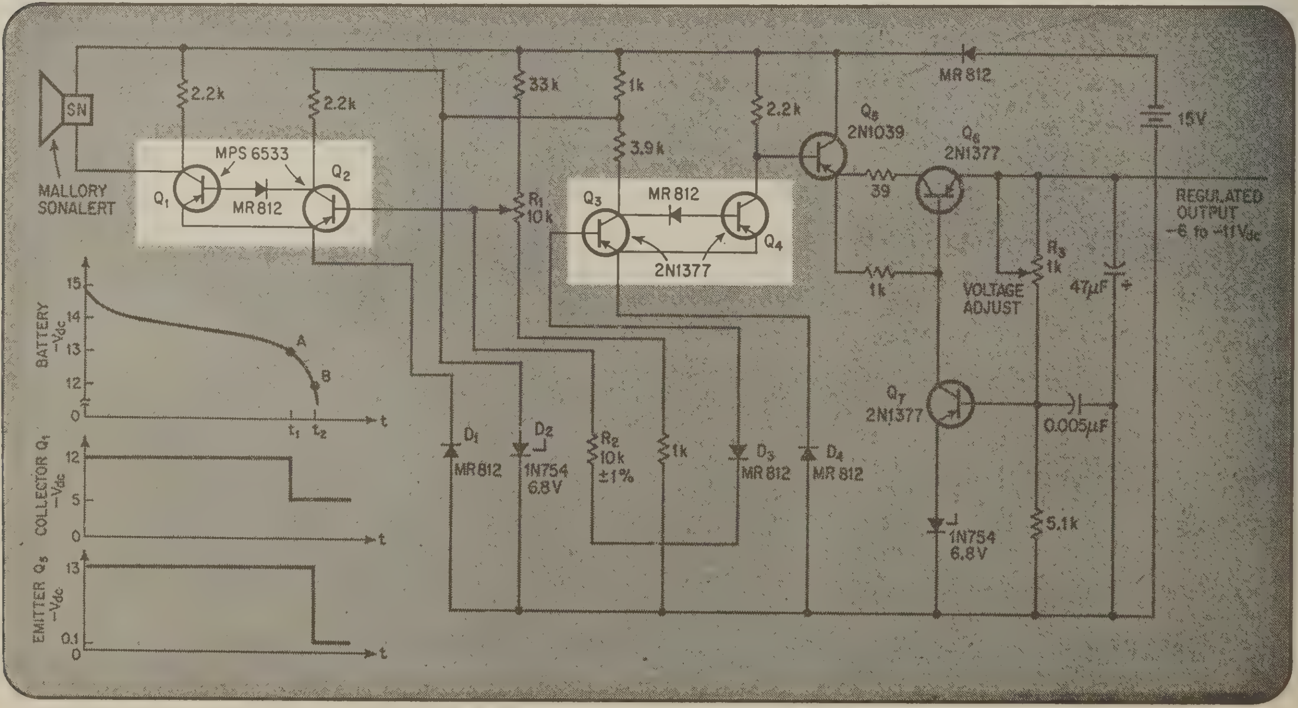
The trigger point of Q_1 — Q_2 is set between —6 and —14 volts dc by adjusting potentiometer R_1. At this point in the battery-discharge curve, Q_2 cuts off. This causes Q_1 to conduct and sound the alarm. The annunciator is a relatively new device that requires only 3 milliamperes at 6 V dc for a full 80-decibel tone output.

As the battery voltage decreases further, the voltage drops across R_2 and D_3 account for the lower trigger voltage presented to the Q_3 — Q_4 switch. At this second cutoff point, the voltage regulator is shut down. When Q_3 — Q_4 switches, Q_5 is cut off, removing battery voltage from the regulator.

The 10-kilohm R_2 makes the second trigger point about 0.50-v lower than the first. R_2 may be varied to change the voltage difference and increase or decrease the time (t_2 — t_1) on the discharge curve This will determine the time between alarm and shutdown. To minimize trigger-point interaction, the two Schmitt triggers are isolated by diode D_3.

With a 15-v battery supply, potentiometer R_2 allows the regular output to be adjusted between —6 and —11 V dc.Regulation is 1%. The entire circuit drains only 25 milliamperes from a fully charged battery, and even with both triggers actuated, the current demand is only 4 mA—low enough to keep the alarm sounding for quite a while.

Early warning. When battery voltage drops to point A on the discharge curve, Q_2 switches on Q_1, activating the alarm. The battery continues to discharge and when point B is reached Q_3 and Q_4 switch, thus cutting off Q_5 and shutting down the voltage regulator section. R_1 and R_2 set the trigger points; R_3 adjusts the regulator output.



Simple photocell circuit measures pulsed laser power

By George Bowman and T. Koryu Ishii
Marquette University, Milwaukee, Wis.

For measuring a pulsed laser's output power, simple circuits using a photovoltaic cell and a voltmeter are impractical because of their low sensitivities and large time constants. Moreover, most pulsed laser outputs are too short to be properly captured and recorded by this type of circuit. A transistor and a switch added to the basic circuit provide a meter indication that's easy to read and, if necessary, the circuit is easy to calibrate.

The design hinges on charging a capacitor to a voltage determined by the intensity of the laser beam striking a photocell. The amount of charge on the capacitor is proportional to the laser's power output.

Initially, the circuit's ganged three-position switch is set to "Measure" and S_1 to "On." When no light strikes the photocell, its resistance is much higher than that of R_1. When a light pulse does strike the cell, its resistance drops, abruptly increasing the voltage across R_1. As a result, a current pulse flows through the emitter-base junction of Q_1, charging the capacitor. As soon as the pulse passes, the photocell's resistance returns to its starting value, trapping the charge on the capacitor.

When S_2 is set to "readout," the capacitor discharges through R_2 and the transistor, which now functions as an amplifier. The meter pointer deflects to some maximum value, which represents the laser power, then slowly returns to its initial point.

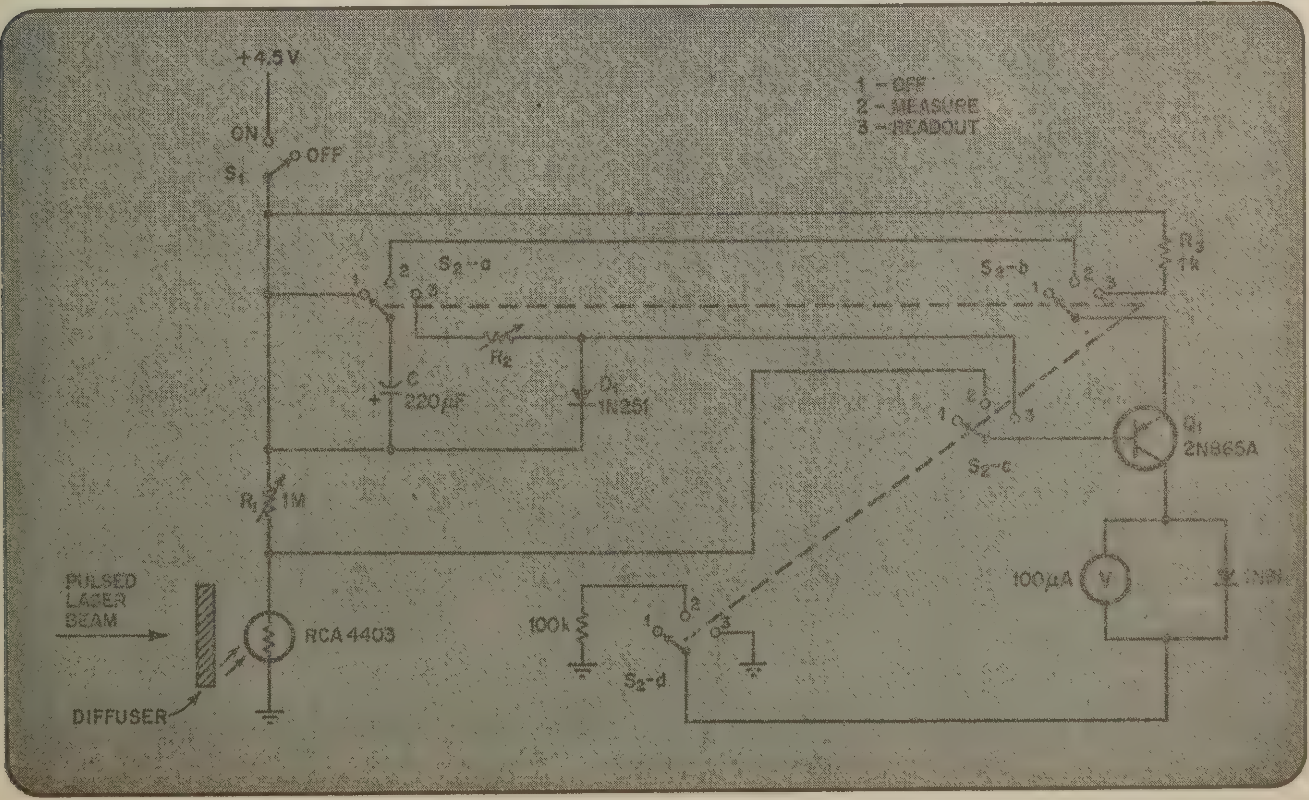
The time constant of R_2 and C should be greater than 350 seconds; R_2 can be adjusted so that the light doesn't cause the meter to read off scale.

Since the maximum deflection is a measure of the power in the light pulse, it's often convenient to prepare a calibration curve for the circuit by plotting maximum deflection against the input voltage to the laser. For precision measurements, the circuit must be calibrated with a lumen meter or a calorimeter.

The photocell is in a sealed chassis, behind a diffuser, usually a piece of frosted glass. The first shields it from ambient light, and the second attenuates the incoming beam. However, light leakage is inherent in the system. To compensate for it, S_1 is set at "On," S_2 at "Measure," and R_1 is adjusted until the meter deflection is closest to zero. Next, S_2 is switched to "Off" to remove stray voltage from C, and then turned back to "Measure," and the circuit is ready.

Diode D_1 and resistor R_3 provides temperature compensation; R_3 also limits the meter current.

A light measure. With S_1 closed and S_2 set to "Measure," the laser pulse is fired at photocell. The cell's resistance drops, causing capacitor C to charge to a voltage proportional to beam power. S_2 is then set to "Readout," which allows C to discharge through the transistor amplifier and the meter.



Regulator gives overvoltage protection for TTL

By T.K. Hemingway
British Aircraft Corp. Ltd., London

Many applications require low-voltage regulators that must be stable and offer overvoltage protection without becoming too complex. In these applications, the conventional zener just won't do, while the voltage regulator that derives its low-voltage output from a much higher input voltage can endanger circuitry if its pass transistor fails.

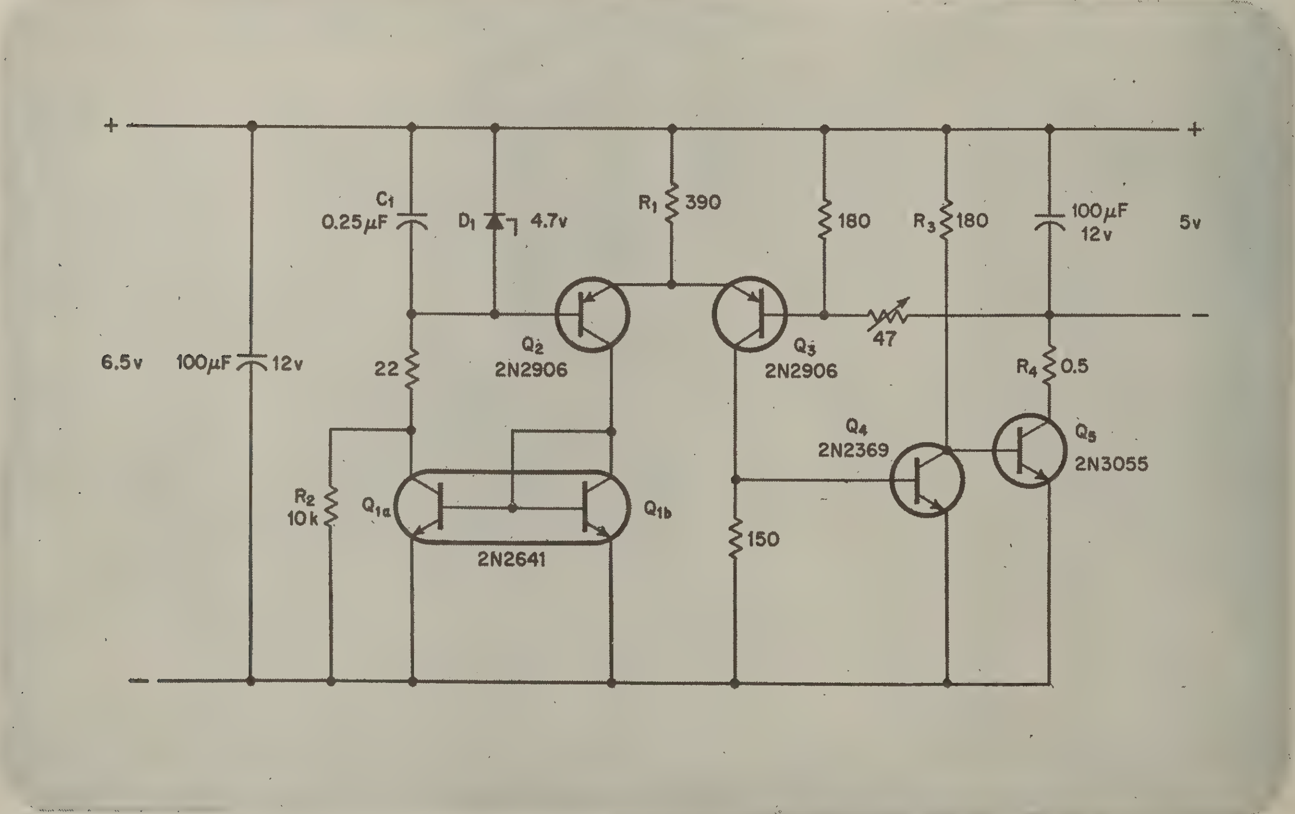
The circuit shown fills both requirements. It provides either 4 or 5 volts at 1 ampere from a 6.5-V supply, depending on the zener diode used, and offers adequate protection against overvoltages. A 3.6-V zener, for example, will give a 4-V output, whereas a 4.7-V zener gives a 5-V output.

Transistor Q_2 acts as a constant current drive for the zener. And adding Q_3 forms a comparator, which, with its associated feedback loop, provides excellent isolation from input variations. With Q_1 acting as a current mirror, the zener can be driven as shown even with a very low input-to-output voltage differential. R_2 is added to assure that the circuit starts; R_3 provides base drive and R_4 limits the transient collector current of Q_5, and C_1 prevents loop oscillations.

The circuit gain at dc is much higher than at first appears. This is because any tendency for the output voltage to fall below the preset level gives Q_2 more of a share of the current through R_1 since the base potential of Q_3 is going more positive. This increases the current in Q_{1b}, which also boosts the current in Q_{1a} and in the zener.

This gain in zener current tends to increase the voltage across the output. The mechanism operates in addition to the normal loop where, as the current through Q_3 decreases due to the assumed drop in output voltage, the current through Q_4 also decreases, allowing more of the current flowing through R_3 to drive Q_5. Therefore Q_5 conducts harder and the output tends to be restored.

Added protection. Circuit provides isolation from input variations and can operate with a very small input-to-output voltage differential. Overvoltage protection is needed only if external voltages reach the output directly, since a series regulator failure is no longer disastrous to external circuits.



Digital bidirectional detector keeps the count honest

By J. van Duijn
Unilever Research Labs, Vlaardingen, The Netherlands

Accurate measurements can be attained by using a set of square-wave detector signals generated by instruments such as optical interferometers, incremental shaft encoders, or moire gratings. The key is a bidirectional scheme that's essentially immune to noise and pulse jitter.

A directional change in the measured value of these signals (A and B in the timing diagram) is indicated by a corresponding change in the 90° phase relationship between them. Direction and number of cycles are sensed by a detector and a bidirectional counter.

The propagation delays through the gating on the set inputs of the up and down J-K sensors assure that per pulse period one of these sensors is set on the first leading edge of signal B. After a quarter cycle, J-K$_1$ or J-K$_3$ is reset by A or $\overline{A}$ on the overriding reset input. Jitter on signal A will result in resetting the appropriate binary on the first logical 0. The only evident restriction for honest operation is that jitter on the edges of A and B does not coincide.

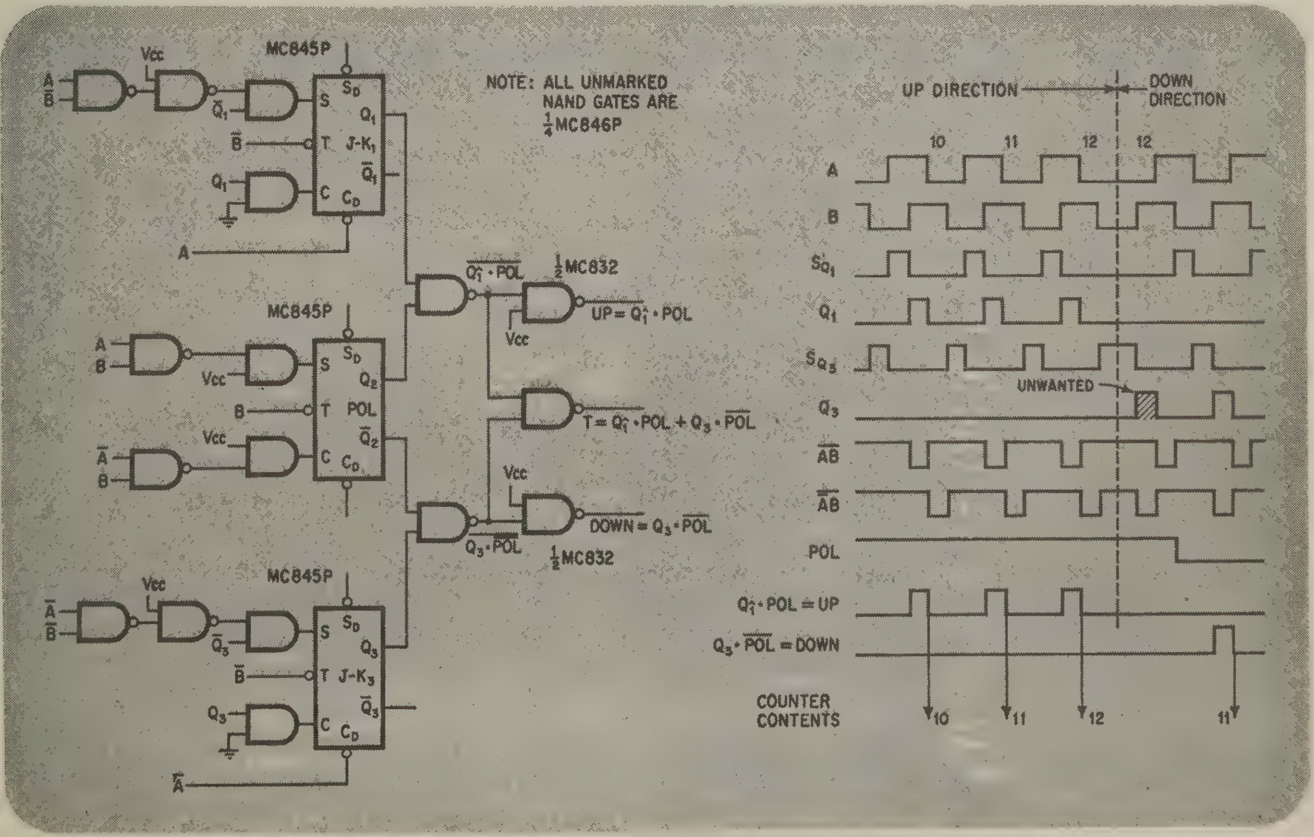
J-K$_1$ will set—that is, Q$_1$ becomes binary 1—if $A = 1$ and $B = 0$ prior to the leading edge of B. The set input remains 1 through the trailing edge of the clock pulse $\overline{B}$ because of delays in the input gate and inverter. In reverse direction, J-K$_3$ turns on when both A and B are 0, prior to B's leading edge.

However, if only J-K$_1$ and J-K$_3$ were used, a systematic error could occur depending on where the direction is reversed. One such case is shown in the timing diagram, where A and B are both 0 before the rise of the first B pulse, so Q$_3$ can turn on and produce an unwanted down pulse. No down pulses should occur until the 12th cycle has been completed.

To prevent such outputs, POL enables or disables the appropriate pulse output line. Since POL is set or cleared by B, which is the complement of the two sensor set inputs, it therefore switches on the trailing edge of B to the state that represents the output pulse to be counted. In effect, it waits for the premature output to subside before allowing that output line to go binary 1. Since Q$_2$ is still high when Q$_3$ first goes high in the example, the down output stays low.

POL is also used for the clock generator, as it allows the center output gate to OR only the valid pulses and provide the correct number of pulses to the bidirectional counter's clock input.

Noise immunity. Delays through the input gates on the J-K flip-flops ensure that the up or down sensor is set on the first leading edge of the B signal in noise systems. J-K$_1$ generates countup pulses; J-K$_3$, countdown units. The POL binary polices the J-K$_1$ and J-K$_3$ outputs to cancel out pulses generated by systematic errors that can occur under reversal.



Wired OR circuit simplifies binary number comparison

By Louis E. Frenzel Jr.
Silver Spring, Maryland

Comparing two multibit binary numbers in a wired OR circuit is both simpler and less expensive than the more common approach of using several exclusive NOR circuits and a NAND gate. The simpler version offers up to a 50% reduction in package count, while the fewer number of gates used improves speed.

The wired OR circuit is basically equivalent to available four-bit medium-scale integrated comparators, but substantially less expensive. A pair of quad two-input NAND gates, such as the 946 (DTL) or the 7401 (TTL), can replace a single package four-bit MSI comparator circuit at less than one-third of its cost.

The circuit operation can be seen by analyzing the related Boolean equations to compare two four-bit numbers, A and B.

$$\text{Equality} = E = (A_1B_1 + \bar{A}_1\bar{B}_1)\,(A_2B_2 + \bar{A}_2\bar{B}_2)\\ (A_3B_3 + \bar{A}_3\bar{B}_3)\,(A_4B_4 + \bar{A}_4\bar{B}_4)$$

Complementing both sides of the equation, then reducing it with DeMorgan's theorem yields:

$$\bar{E} = \overline{(A_1B_1 + \bar{A}_1\bar{B}_1)} + \overline{(A_2B_2 + \bar{A}_2\bar{B}_2)} + \overline{(A_3B_3 +}\\ \overline{\bar{A}_3\bar{B}_3)} + \overline{(A_4B_4 + \bar{A}_4\bar{B}_4)}$$

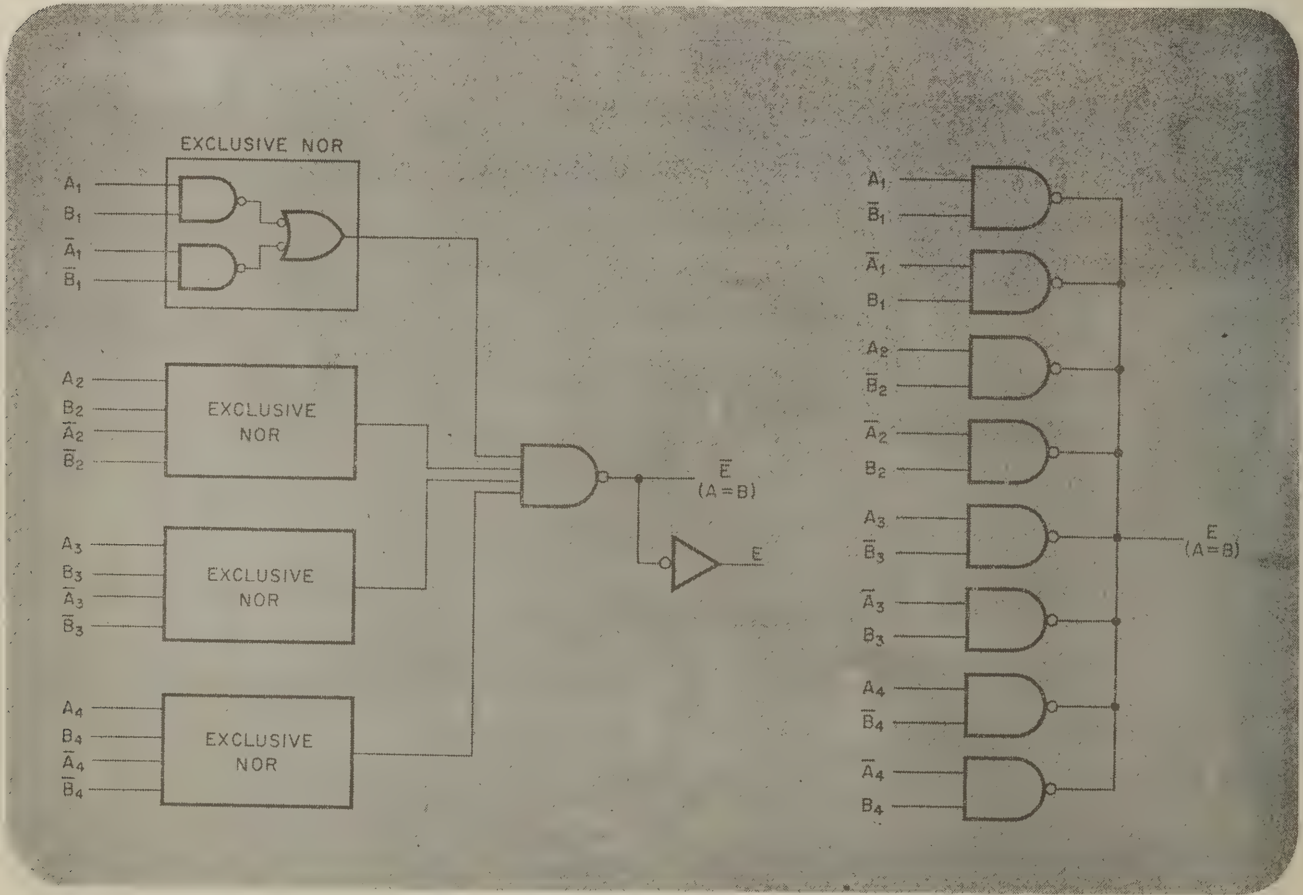
Since $\overline{AB + \bar{A}\bar{B}} = A\bar{B} + \bar{A}B$, the equation becomes:

$$\bar{E} = A_1\bar{B}_1 + \bar{A}_1B_1 + A_2\bar{B}_2 + \bar{A}_2B_2 + A_3\bar{B}_3 +\\ \bar{A}_3B_3 + A_4\bar{B}_4 + \bar{A}_4B_4$$

Again, complementing both sides of the equation expresses the output of the wired OR circuit:

$$E = \overline{A_1\bar{B}_1 + \bar{A}_1B_1 + A_2\bar{B}_2 + \bar{A}_2B_2 + A_3\bar{B}_3 +}\\ \overline{\bar{A}_3B_3 + A_4\bar{B}_4 + \bar{A}_4B_4}$$

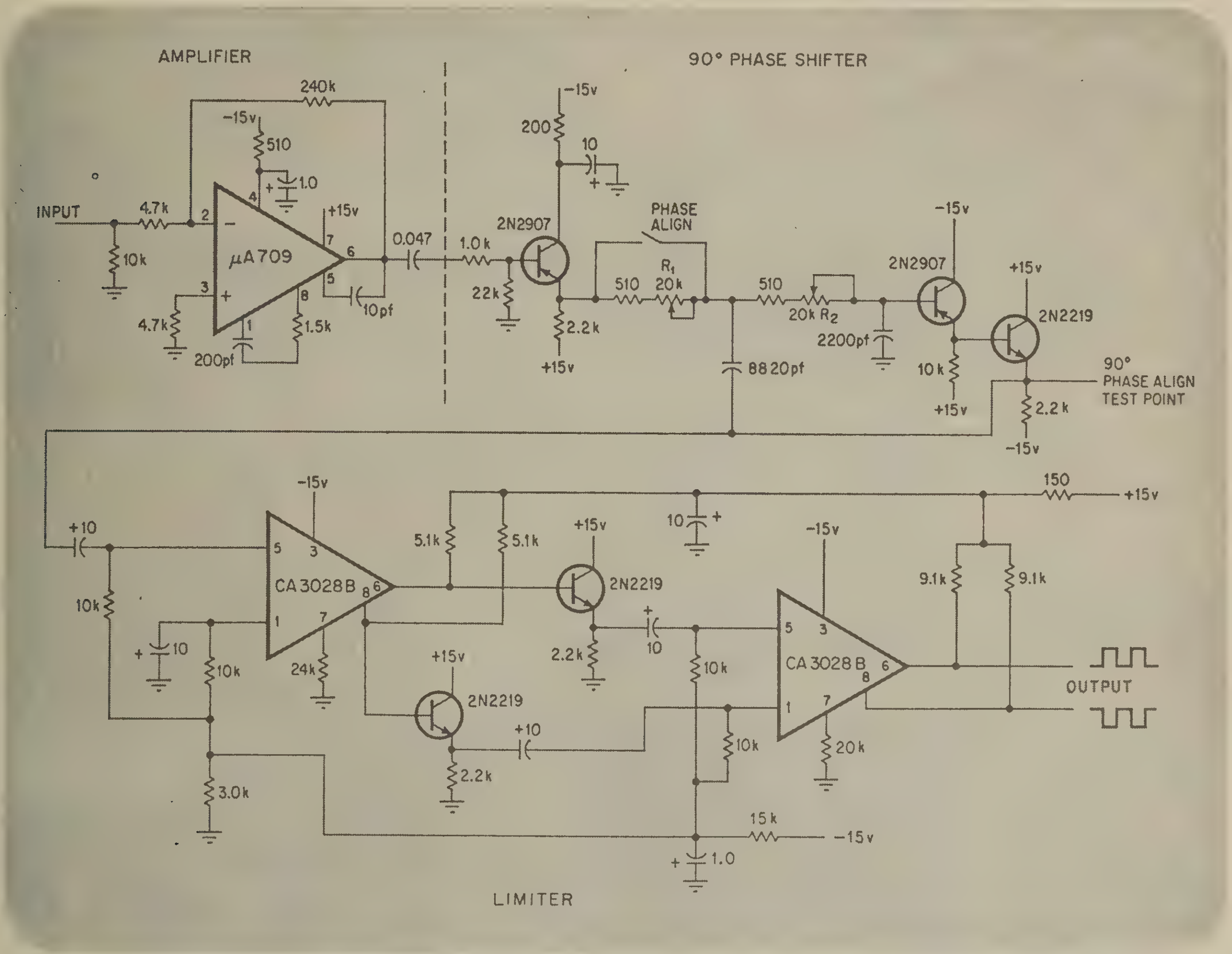
Logically better. Commonly used circuit (left) requires substantially more gates to compare two multibit binary numbers than does the wired OR circuit (right). Latter configuration is faster than the exclusive NOR approach and can be constructed of two quad two-input gates, such as the 946 (DTL) or the 7401 (TTL).



IC limiter preserves phase over 50-dB dynamic range

By Roland J. Turner
RCA Missile and Surface Radar division, Moorestown, N.J.

Insensitive. The limiter circuit provides symmetrical complementary outputs that are in phase quadrature with the input signal over 50-dB dynamic range. Using two inexpensive ICs the limiter generates a 15-V peak-to-peak signal that lags the input signal by 90°, and remains in quadrature within ± 0.5°.



Operation of frequency- and phase-modulated systems will be impaired by any phase shift in the processing circuitry. For example, serious errors will occur if the phase shift in the limiter circuit used with composite video, or zero crossing detectors changed with either the amplitude or frequency of the incoming signal. In addition, double-sideband systems generally require accurate phase references that must be supplied in quadrature for both the modulation and demodulation sections.

Two inexpensive integrated circuits can be used to build a circuit that provides two limited complementary outputs (each in phase quadrature with the input signal) that track the phase to the input signal to within ±0.5°. The circuit is insensitive to changes in input signal amplitude from 0.5 to 100 millivolts peak-to-peak and provides a limited output swing of 15 volts peak-to-peak between 2 and 60 kilohertz.

This circuit, in addition to limiting the signal with little phase error, provides a quadrature phase shift essential in operating a conventional phase detector. It also provides complementary output signals required to drive MOSFET switches in a balanced phase detector. Moreover, its symmetrical outputs prevent generation of unwanted dc and video pedestals in the phase-detector output.

The complete circuit comprises an operational amplifier, a 90° phase shifter, and the limiter. Although the amplifier design is straightforward, the method used to obtain the 90° phase shift isn't.

The phase shifter stage employs an active low-pass filter with a Chebyshev response. This provides a 90° phase shift at the corner frequency where the amplitude response is unity, a feature unattainable with a two-pole resistive-capactive passive network. Adjustment of R_1 and R_2 yields a 90° phase shift for any corner frequency between 2 and 60 kHz.

The limiter uses two RCA CA3028B differential amplifiers. To achieve symmetrical limiting over a wide dynamic range the dc path from pins 1 and 5 must be equal and must return to the same bias supply. The limiter stages must be driven from a low source resistance, such as an emitter follower. Lower phase distortion also is obtained if the CA3028Bs are operated from a 1.0- to 1.25-milliampere current source.

Optoelectronic switch monitors line power

By James van Zee,
Harvard University, Cambridge, Mass.

A simple optoelectronic switch can be used to detect a power-supply failure and relay the message to a digital shut-down circuit. The switch's low-level logic circuit is completely isolated from the power mains by optical coupling. What's more, it's inexpensive—total parts for the circuit shown cost about $7—and is easily adapted to monitor any ac or dc supply. This version plugs into 110-volt or 220-volt ac lines, depending on the size of series resistor R_1.

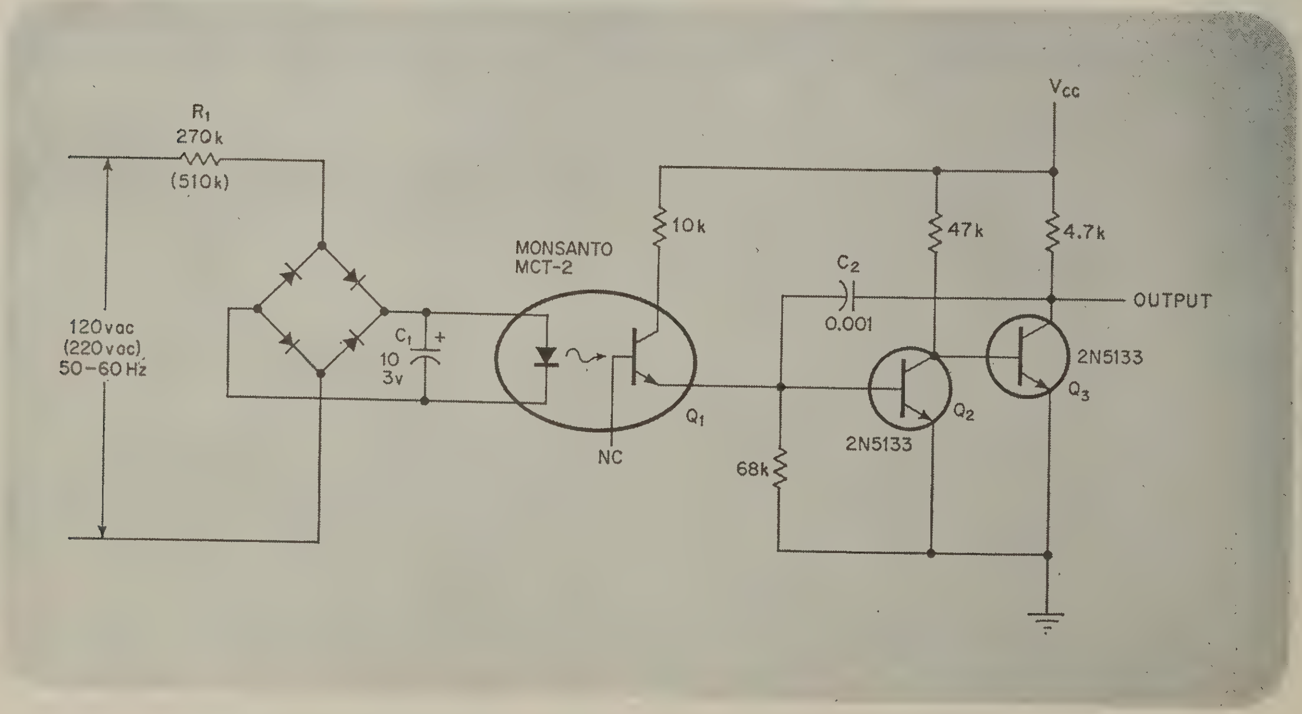
When line power is normal, the diode rectifier and capacitor C_1 provide the minimum current of about 200 microamperes required to keep the light-emitting diode lit. In turn, the LED holds phototransistor Q_1 in saturation, so that the output is a logical 1. If the line voltage goes down, Q_1 switches off; the output pair Q_2-Q_3 drops the output level to logical 0 (ground), setting flip-flops in a shut-down circuit.

Response to a power failure typically is within 2 milliseconds, fast enough for shutdown. The circuit is insensitive to normal zero crossings of the ac voltage. The capacitor, C_1, supplies enough current to let the LED keep Q_1 on during these few milliseconds.

However, response time varies somewhat with the dc current gain of Q_1. A device with a more tightly specified current gain than the switch shown should be used in applications where operating temperature will vary widely. Also, shutdown logic, such as some TTL circuits, may ring if the output transitions are not shaped. Capacitor C_2 prevents this.

The large series resistance allows use of inexpensive, low-voltage diodes in the input circuit. Total circuit power consumption is about 50 milliwatts.

Optoelectronic plug. Low-level logic monitors power failures through phototransistor Q_1. As long as line power is normal, the light-emitting diode saturates Q_1, which holds the output at logical 1. A power failure turns off the optoelectronic switch, causing the output to drop to the logical 0 level.



Symmetry principle eases design of summing op amp

By Brock Dew
MIT, Cambridge, Mass.

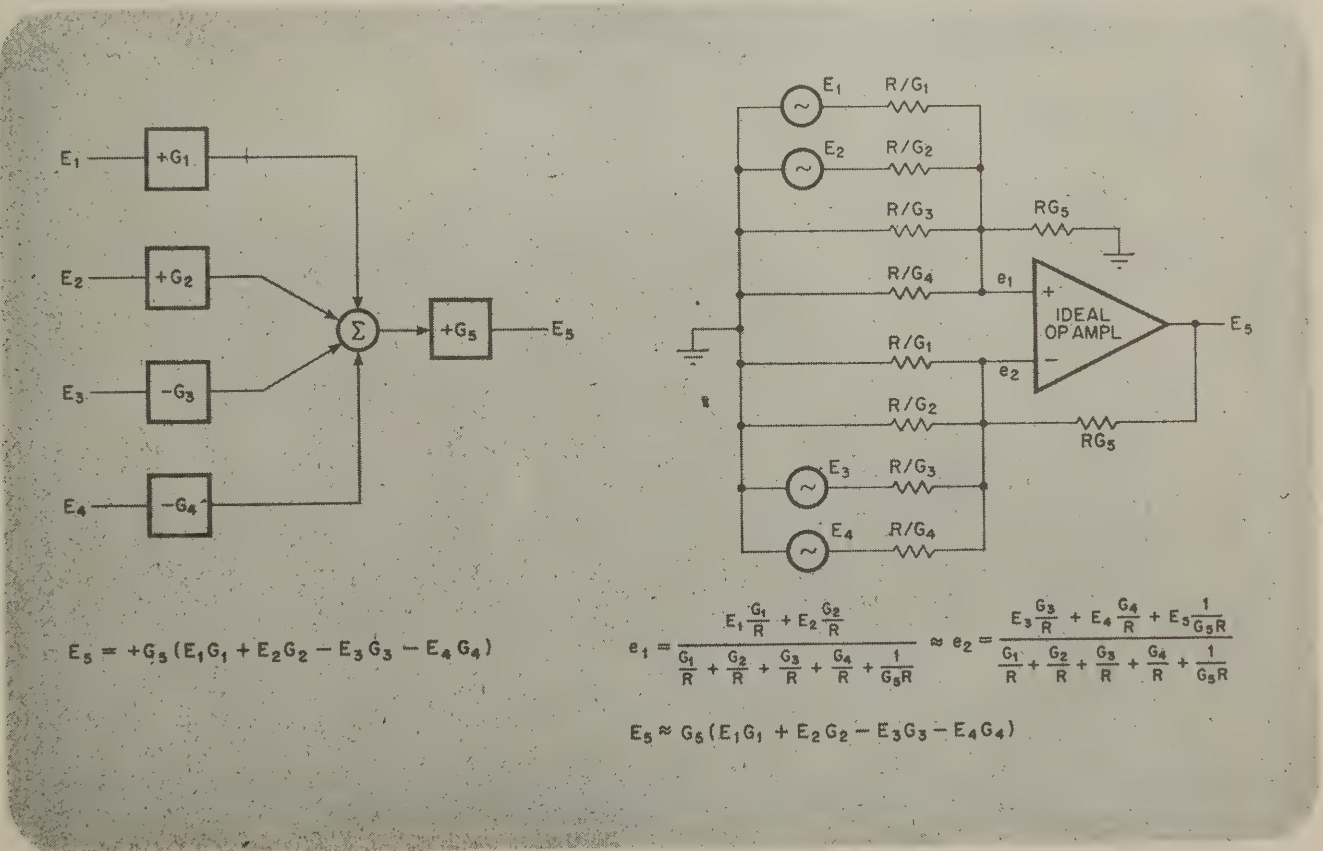
Computing resistor values for differential summing of voltages into operational amplifiers needn't be complicated if the principle of symmetry is employed. With this technique the task is accomplished virtually by inspection—even when several signals must be weighted with different gains and polarities. Moreover, this method can be extended to reactive elements, such as capacitors, in design summing integrators and filters. And scaling is easier because a single gain multiplying the sum allows over-all gain to be changed easily.

First, select a base value of resistance, R, usually 20 kilohms for IC op amps. The signals then are summed through resistors whose admittance is proportional to the desired weighting, and whose connection to the op amp depends on polarity. A resistor whose admittance is proportional to the reciprocal of the over-all gain weights the feedback. Weighting is accomplished by selecting the absolute magnitude of the desired gains, G.

Note that for every resistor weighting an input or feedback signal, a complementary resistor must be added to ground on the other side of the differential op amp. This is required to maintain symmetry.

The differential op amp action drives e_2 until it almost equals e_1. This permits modeling to be realized. Both individual and over-all gains should be apportioned to prevent e_1 and e_2 from exceeding the amplifier's common-mode operating range. Maintaining resistor symmetry also equalizes the dc resistance to ground at the two op amp inputs, and minimizes offsets due to leakage current. It also tends to balance the two inputs' sensitivity to pickup and prevents amplifier input impedance from affecting the validity of the summing equations.

Simple summing. System block diagram (left) demonstrates weighting of signals with gains of either polarity. Circuit diagram (right) shows that feedback is weighted with a resistance proportional to over-all gain; the summing resistor values are inversely proportional to absolute magnitude of desired gains.



$$E_5 = +G_5(E_1G_1 + E_2G_2 - E_3G_3 - E_4G_4)$$

$$e_1 = \frac{E_1\frac{G_1}{R} + E_2\frac{G_2}{R}}{\frac{G_1}{R} + \frac{G_2}{R} + \frac{G_3}{R} + \frac{G_4}{R} + \frac{1}{G_5R}} \approx e_2 = \frac{E_3\frac{G_3}{R} + E_4\frac{G_4}{R} + E_5\frac{1}{G_5R}}{\frac{G_1}{R} + \frac{G_2}{R} + \frac{G_3}{R} + \frac{G_4}{R} + \frac{1}{G_5R}}$$

$$E_5 \approx G_5(E_1G_1 + E_2G_2 - E_3G_3 - E_4G_4)$$

Single IC pulser eliminates contact bounce

By A. James Laurino
Cambridge, Mass.

Contact bounce encountered when mechanical switches are interfaced with high-speed logic circuits can cause errors. An economical anti-bounce circuit using a single integrated circuit does the job without large, expensive filter capacitors.

The circuit comprises a quadruple dual-input positive NAND gate; gates 3 and 4 form a set-reset flip flop.

When a break-before-make switch is in the normally closed position, one input to gate 3 is grounded and the voltage to gate 1 is positive. This causes the output of gate 3 to go low and the output of gate 1 to go high. Thus, with one input to gate 2 high and the other low, the gate's high.

When the switch is reversed, one input to gate 3 rises to a positive voltage and the input to gate 1 goes to zero. This causes the output of gate 3 to remain high and the output of gate 1 to go high. With both inputs to gate 2 high, its output goes low, thus initiating the pulse.

The pulse's leading edge then resets the flip flop, which causes gate 3's output to go low until the switch again is returned to the normally closed position. When gate 3's output goes low, gate 2's output is forced to go high, and the pulse is discontinued.

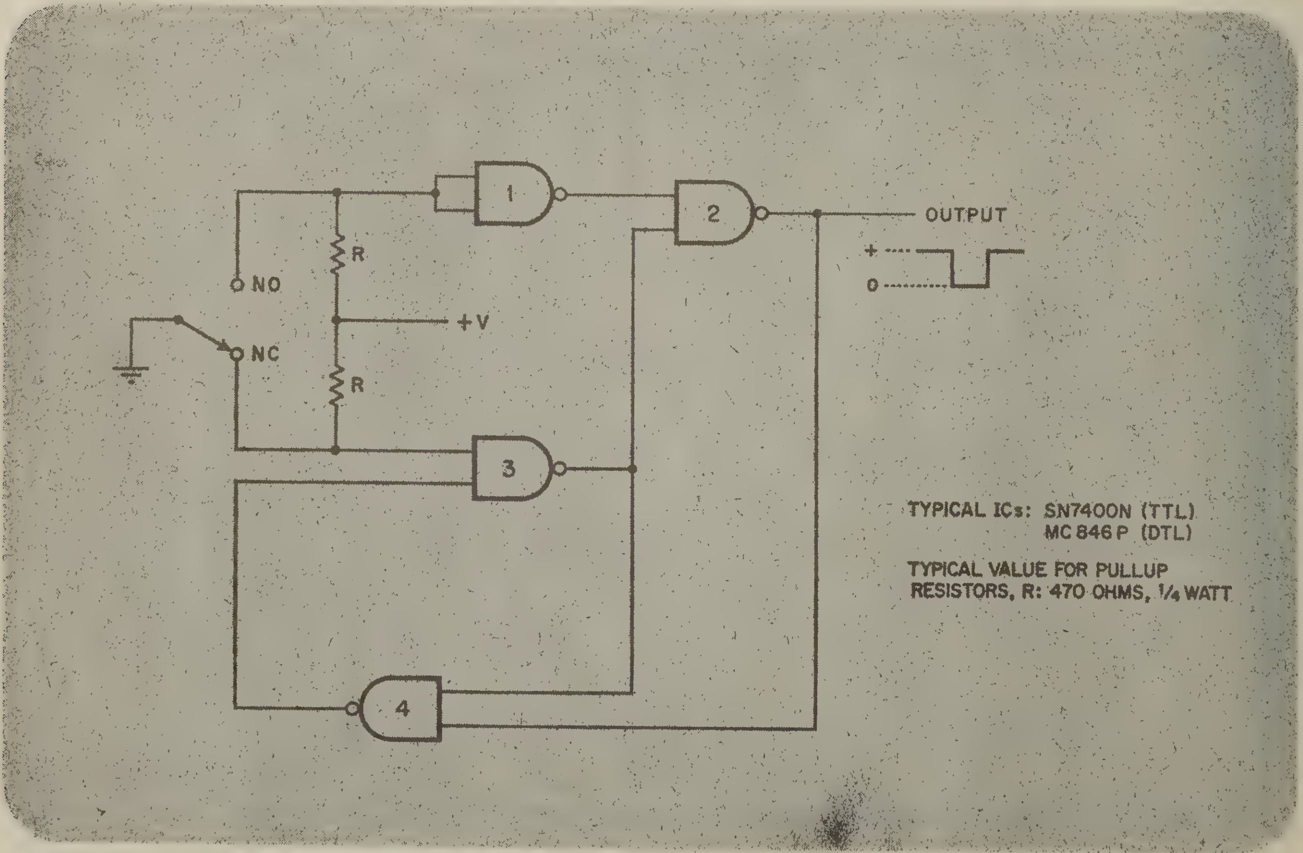
Since the pulse is completed within a time much shorter than the period of one contact bounce, the circuit is desensitized to any changes at the output of gate 1. Thus the effect of contact bounce is eliminated. Of course, it's assumed that contact bounce is about one contact and never between two.

When the switch is returned to the normally closed position, the input to gate 1 first rises to positive voltage, causing its output to go low, followed by one input of gate 3 going to ground. This sequence, which results from the break-before-make action of the switch, prevents a false output.

Pulse width is determined by the time it takes the pulse's leading edge to propagate from the output of gate 2 through gates 4, 3 and 2. To lengthen the pulse width, a capacitor must be connected from the output of gate 4 either to the input of gate 3, if TTL circuitry is used, or to ground if DTL is used. A 220-picofarad capacitor provides a 150-nanosecond pulse.

Testing the circuit is quite simple. With the input of gate 3 disconnected from the switch and connected to the output of gate 1, a square wave applied to the input of gate 1 should produce an output pulse.

Bounceless. This circuit produces a negative-going pulse whose minimum width is approximately equal to three gate delays. The pulse width, however, can be increased by adding a capacitor. If a TTL IC is used, the capacitor is placed between the outputs of gate 4 and gate 3; for DTL, it's connected from the output of gate 4 to ground


1
2
OUTPUT
+
0
R
NO
+V
NC
R
3
4
TYPICAL ICs: SN7400N (TTL)
MC 846 P (DTL)
TYPICAL VALUE FOR PULLUP RESISTORS, R: 470 OHMS, 1/4 WATT

Zener diodes reset sampling gate automatically

By Ronnie W. Camp
Georgia Tech, Atlanta, Ga.

With their low impedance when conducting, zener diodes make fine candidates for diode gate samplers where simple structure and low power consumption are desired. Power is consumed only during sampling, and the gate automatically resets at the end of the sampling pulse when the zeners turn off. Furthermore, because of the low series on impedance, only relatively short sampling times (as low as 0.25 microsecond) are needed to acquire new samples.

A gate pulse of proper magnitude and polarity delivered to the primary winding of the balanced transformer reverse biases the zener diodes into breakdown and forward biases the signal diodes. The peak current, I_p, depends on the applied voltage and the series resistance of the transformer primary.

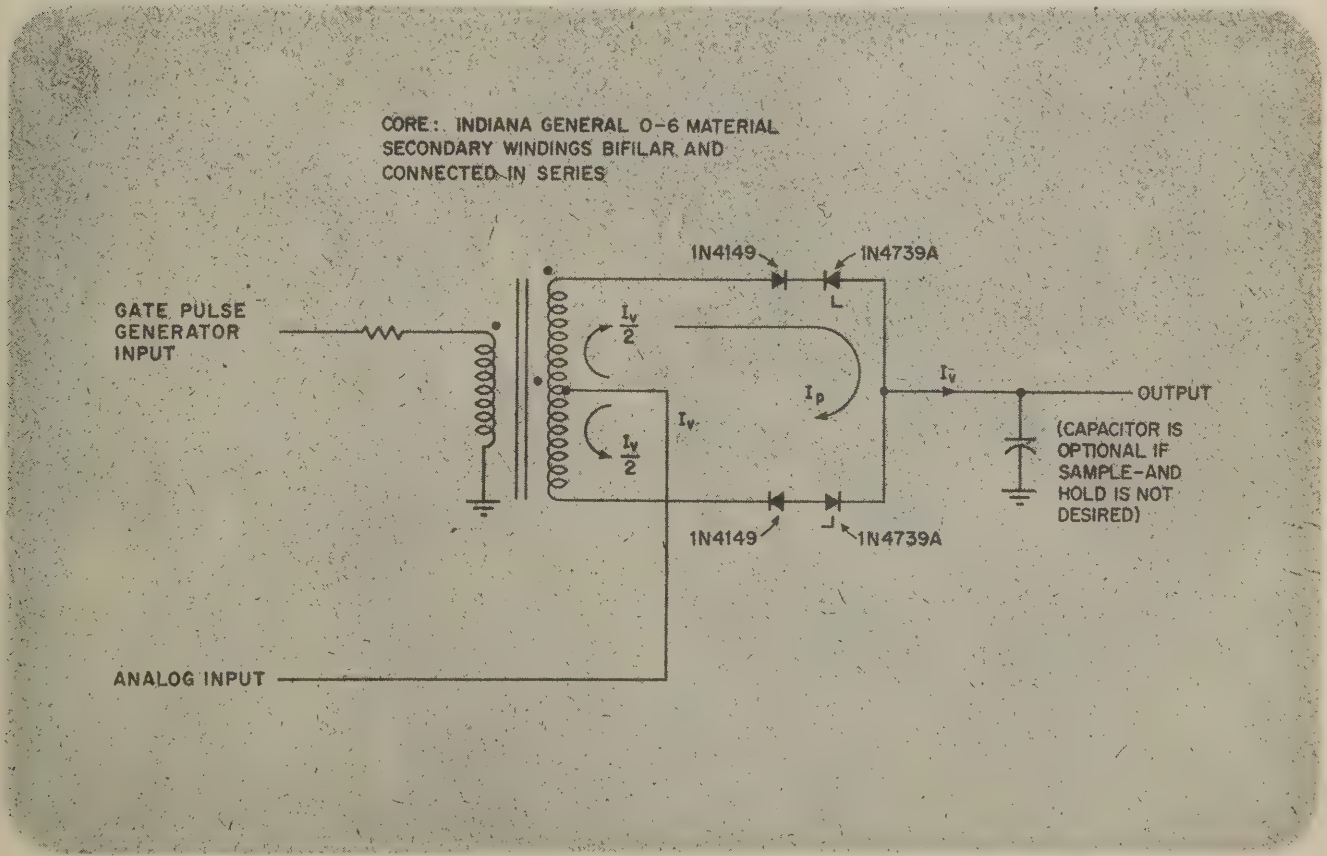
When all diodes are conducting the impedance around the secondary loop becomes quite small. Equal voltages are generated on both sides of the balanced transformer secondary. If the diode voltages are well matched, the output terminal is effectively connected to the analog input. Impedance usually is a few ohms when 6- to 9-volt zeners and high-conductance signal diodes are used.

For most 6-V-or-greater zeners, reverse leakage is low enough to allow long retention of the sample on the output capacitor without significant loss. If the signal and zener diodes are well matched, very low offset can be realized at the output with minimal sampling pulse feedthrough.

When wideband analog signals are handled, the diodes' parasitic capacitance will allow some feedthrough of the analog input, which ultimately limits maximum operating frequency. This is especially true when operated with a fairly high impedance-resistive load. Typical zero bias capacitance values for the zeners are in the tens of picofarads.

In addition to sampling and sample-and-hold circuits, the gate also can be used as a shunt switch, where it has performed well because of the very low diode impedances. Typical peak gating currents in the 100-milliampere range have been used for the 1N4739A, a 9.1-V zener. The 1N4149 signal diode was selected because it has very low forward impedance at the selected gating currents.

Direct route. A sampling pulse at the input to the transformer's primary reverse biases the zener diodes and forward biases the signal diodes, resulting in very low on-impedance for the transformer's secondary loop. The analog input is effectively connected to the output until the sampling pulse is terminated.


CORE: INDIANA GENERAL O-6 MATERIAL SECONDARY WINDINGS BIFILAR AND CONNECTED IN SERIES
1N4149
1N4739A
GATE PULSE GENERATOR INPUT
$\frac{I_v}{2}$
I_v
I_p
$\frac{I_v}{2}$
I_v
OUTPUT
(CAPACITOR IS OPTIONAL IF SAMPLE-AND HOLD IS NOT DESIRED)
1N4149
1N4739A
ANALOG INPUT

Pulse generator uses digital ICs

By Edmund Lafko
Tampa, Fla.

A wide variety of pulse waveforms can be produced with just a few integrated circuits. Such circuits should prove more economical than buying a complete function generator, particularly if the user doesn't require the full capability of the generator. And, if he's in a hurry, putting together a simple pulse generator from available ICs insures prompt delivery.

The circuit comprises five IC flatpacks. Two RD221s are used as a four-bit counter that's driven from an astable multivibrator. The free-running multivibrator uses a single flatpack, an RD209 dual line driver; capacitively coupling the output back to the input provides the feedback path required for oscillation. The four stages of the counter are gated by two RD209 ICs, one of which also provides the inverted output. The switch setting and the output terminal used determine the duty cycle and pulse width of the output waveform.

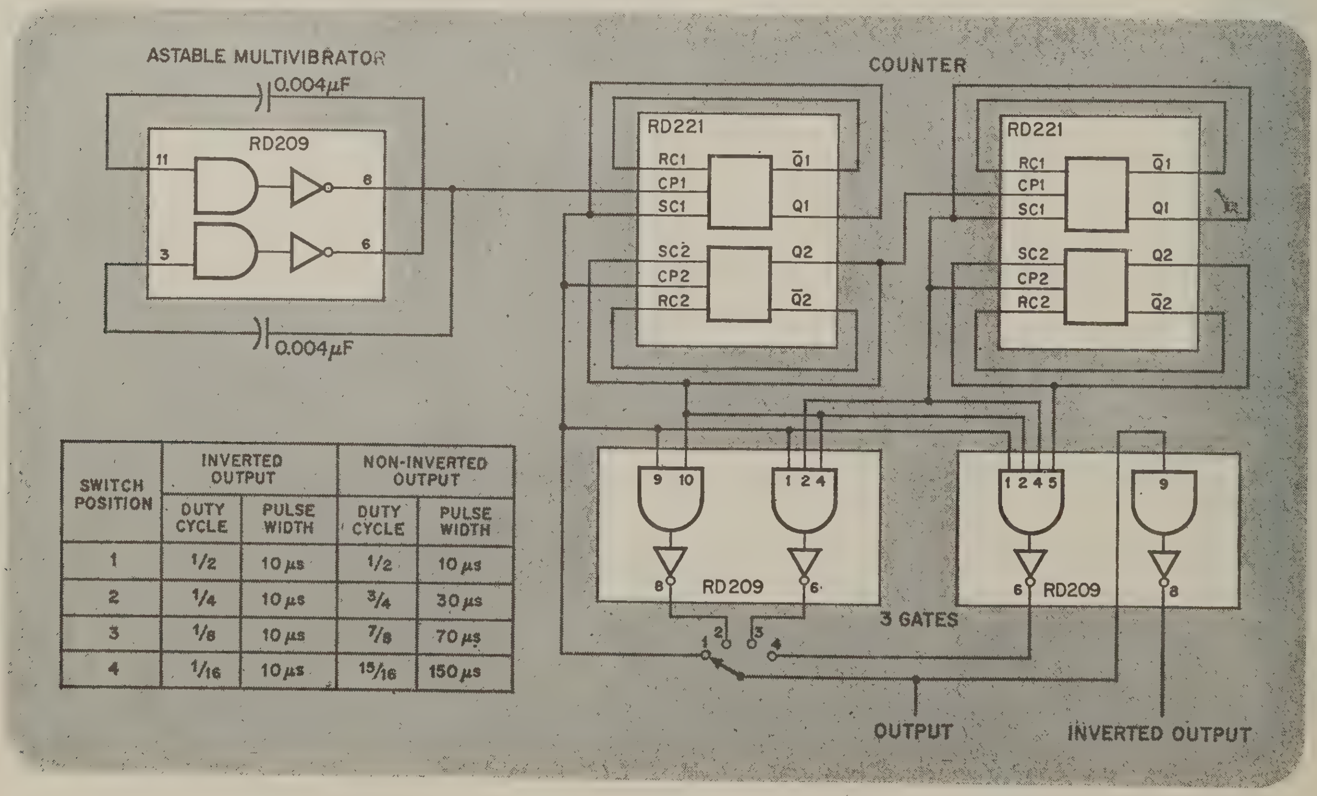
For the example shown, the dual line driver was connected so that the repetition rate was 100 kilohertz. This produces a symmetrical square wave of 10 microseconds at the first stage of the counter. Further processing of the square wave provides a waveform with different duty cycles and a 10 μs pulse width; varying duty cycles with pulse widths of 10 μs, 30 μs, 70 μs, and 150 μs.

By changing the repetition rate of the counter and gating the counter stages, waveforms of various pulse widths and duty cycles, as well as groups of pulses, can be obtained.

This circuitry also could be used as a trigger delay. The delayed trigger pulse would be gated where required within a cycle of the counter.

If the power output isn't sufficient, the circuit can be used to drive additional ICs. Or, if still more power is required, a transistor could be switched by the IC circuit. The voltage, impedance, and rise and fall times of the output can be tailored to meet the individual's specification.

User's choice. An astable multivibrator drives a four-bit counter, which is triggered by the three gates. Numerous waveforms of different duty cycles and pulse widths are obtained simply by selecting the proper switch setting and output terminal. The various combinations obtained with this circuit are detailed.



SWITCH POSITION	INVERTED OUTPUT		NON-INVERTED OUTPUT	
	DUTY CYCLE	PULSE WIDTH	DUTY CYCLE	PULSE WIDTH
1	1/2	10 μs	1/2	10 μs
2	1/4	10 μs	3/4	30 μs
3	1/8	10 μs	7/8	70 μs
4	1/16	10 μs	15/16	150 μs

Voltage monitor is easy on both battery and budget

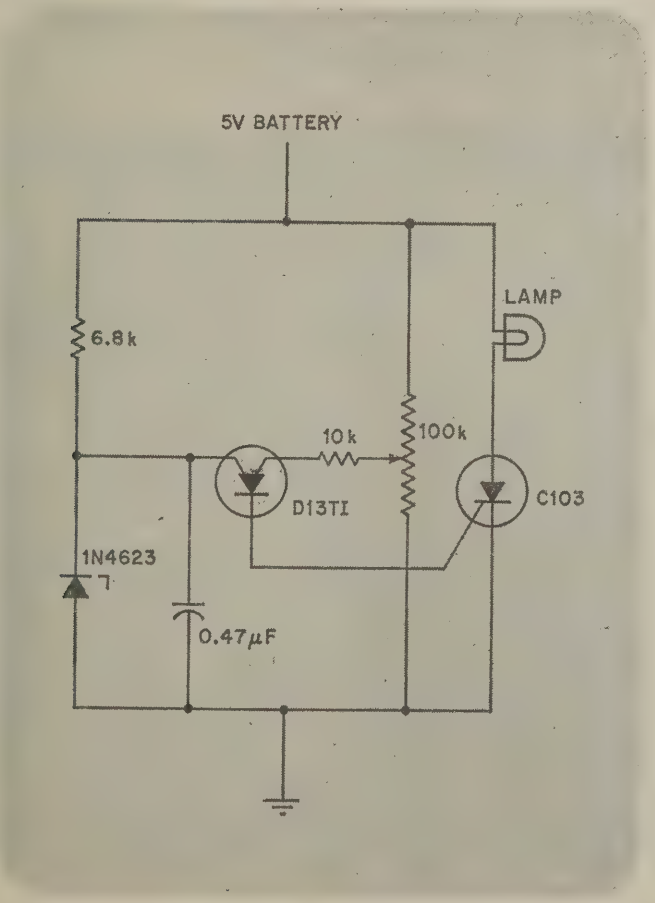
By William G.S. Brown and Victor K.L. Huang
University of Virginia, Charlottesville

At less than $6, even the most tightly budgeted researchers can afford to build this voltage monitor. It is valuable for monitoring critical battery levels during experiments.

The lamp, of course, also goes on when the battery needs replacing or recharging. The voltage across the capacitor triggers the programable unijunction transistor, PUT, at a threshold voltage, which is preset with the variable resistor. The PUT, in turn, fires the silicon controlled rectifier. The PUT consumes very little current and probably good flexibility in threshold voltage adjustment.

If the battery is in good condition, current flows only through the variable resistor and zener diode, plus whatever small leakage currents are present. A low-current zener keeps total current drain within 300 microamperes. Until the PUT fires to start the SCR, neither consume any current.

Battery saver. Voltage monitor drains little battery current. At a preset threshold the transistor turns on the SCR and the lamp. General Electric or equivalent devices can be used.



Optical biasing maintains phototransistor sensitivity

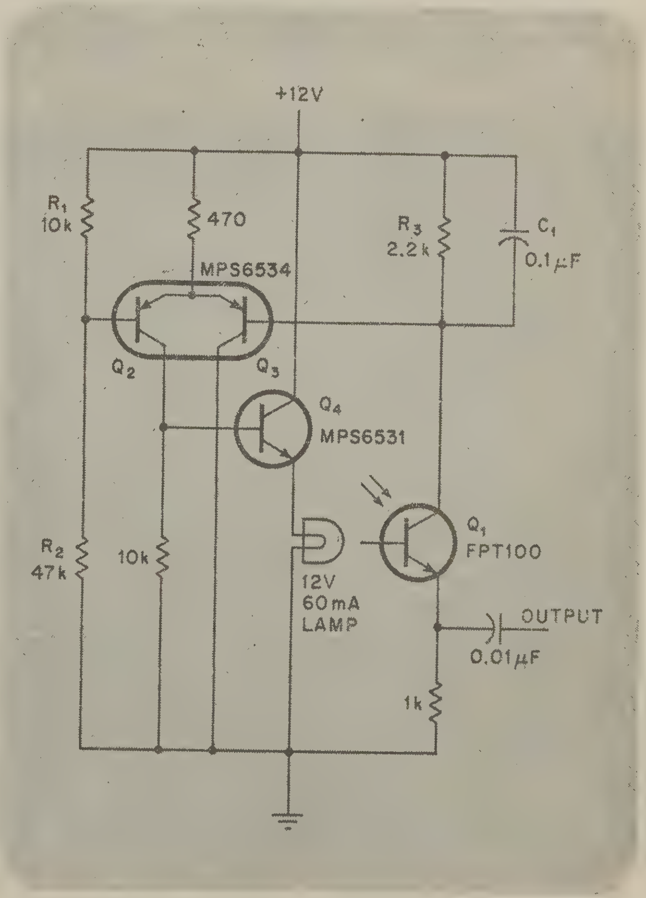
By Dennis Knowlton
University of Wyoming, Laramie

Light-biasing a phototransistor permits it to measure changes in low light levels at high speed. The extra light improves response time by boosting the collector current so that the device operates in a more favorable region. And, unlike in an electrical bias connection to the base, the transistor's sensitivity is not degraded.

The biasing circuit is an electro-optical feedback loop controlling the collector current in phototransistor Q_1. A reference current determined by R_1 and R_2 is compared in differential amplifier Q_2-Q_3 with Q_1's collector current. The amplifier output drives emitter-follower Q_3 to regulate the lamp. The light from the lamp controls the phototransistor's collector current, closing the current control feedback loop.

Bypass capacitor C_1 on the collector resistor prevents feedback to the base of Q_3 (common-collector connection). And the lamp is located where it won't shadow Q_1's active sensitivity cone.

No connection. Leaving Q_1's base unconnected gives it maximum sensitivity to light changes. Collector current is raised by the lamp to improve the response time.



Thermistor stabilizes Gunn oscillator

By T.V. Seling
University of Michigan, Ann Arbor

Gunn-diode oscillators usually take 30 to 40 minutes to warm up and become temperature stable. During this time, a thermistor in the voltage-biasing network that tunes the diode will compensate for resonant cavity changes and quickly stabilize the frequency. In addition, it will reduce frequency drift due to changes in ambient temperature.

The biasing circuit at the left, below, stabilizes an 8-gigahertz oscillator to better than 4 ppm/°C after only a 4-minute warmup. Two general purpose versions of the circuit are shown at the right. The component values and direction of changes in the bias voltage with temperature will depend on the particular oscillator.

Normally, the oscillation frequency decreases as temperature increases because the cavity expands and lowers the resonance frequency. Eventually, the heat from the diode brings the cavity's larger thermal mass to a fairly stable temperature. During warmup, the bias circuit should be compensated for this.

The circuit at the left has a negative temperature coefficient. Measurement of the uncompensated oscillator showed an approximately linear change of —9 megahertz/volt over the biasing range of 8.6 to 10.0 V. The uncompensated circuit drifted —0.8 MHz/°C, had a maximum variation in power output of 0.2 decibel, and took 40 minutes to stabilize.

The oscillator is a Monsanto Electronics DC1414A diode in a coaxial cavity 2.5 inches long. An X-band waveguide forms the outer cavity wall, and the center conductor that holds the diode is brass.

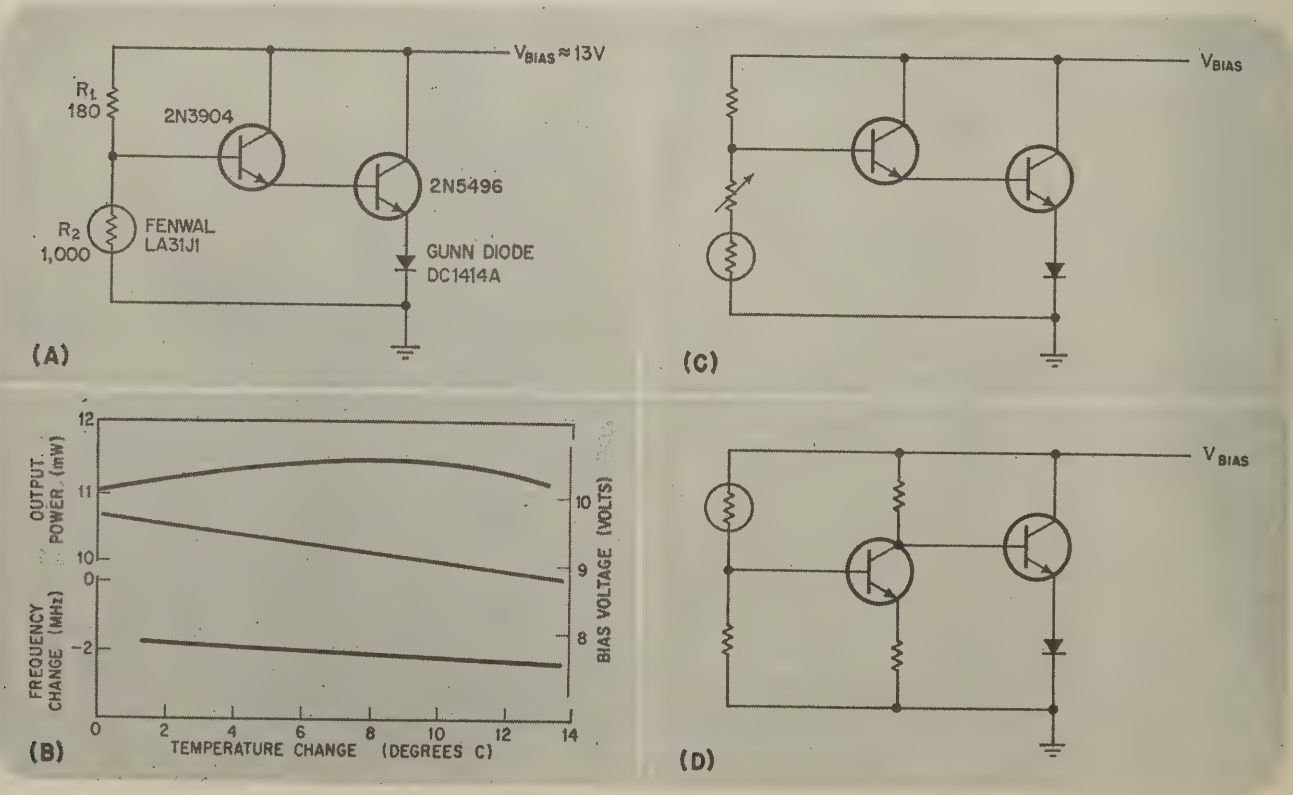
The combination of the resistor R_1 and the thermistor R_2 in the first circuit provides a bias voltage with the negative temperature coefficient.

A Darlington-connected emitter follower furnishes the power gain to drive the diode. The emitter follower was used rather than a directly connected bias network to reduce the amount of heat dissipated in the bias network.

Stabilities of the compensated oscillator are plotted in the graph. After a 4-minute warmup, drift drops to —0.03 MHz/°C. Power output still varies 0.2 dB but becomes stable after the full warmup.

Other oscillators with different temperature coefficients may require padding by a variable resistor to reduce the bias variation. If a greater variation is desired, it can be obtained by using the connection in the third circuit to amplify the bias voltage.

Gunn stabilizer. Thermistor reduces bias voltage when temperature rises, stabilizing diode oscillation frequency. Circuit (A) for an 8-GHz oscillator yields the temperature characteristics charted in (B). Circuit (C) is a version that reduces the bias variation, while the additional gain of (D) provides larger bias swings with temperature.



Op amps form self-buffered rectifier

By Jerald Graeme

Burr-Brown Research Corp., Tucson, Ariz.

A new design for a precision full-wave rectifier uses two operational amplifiers and two diodes and eliminates the need for a buffer. Self-buffering occurs because the input signal sees the high common-mode input resistances of the amplifiers rather than the conventional summing resistors.

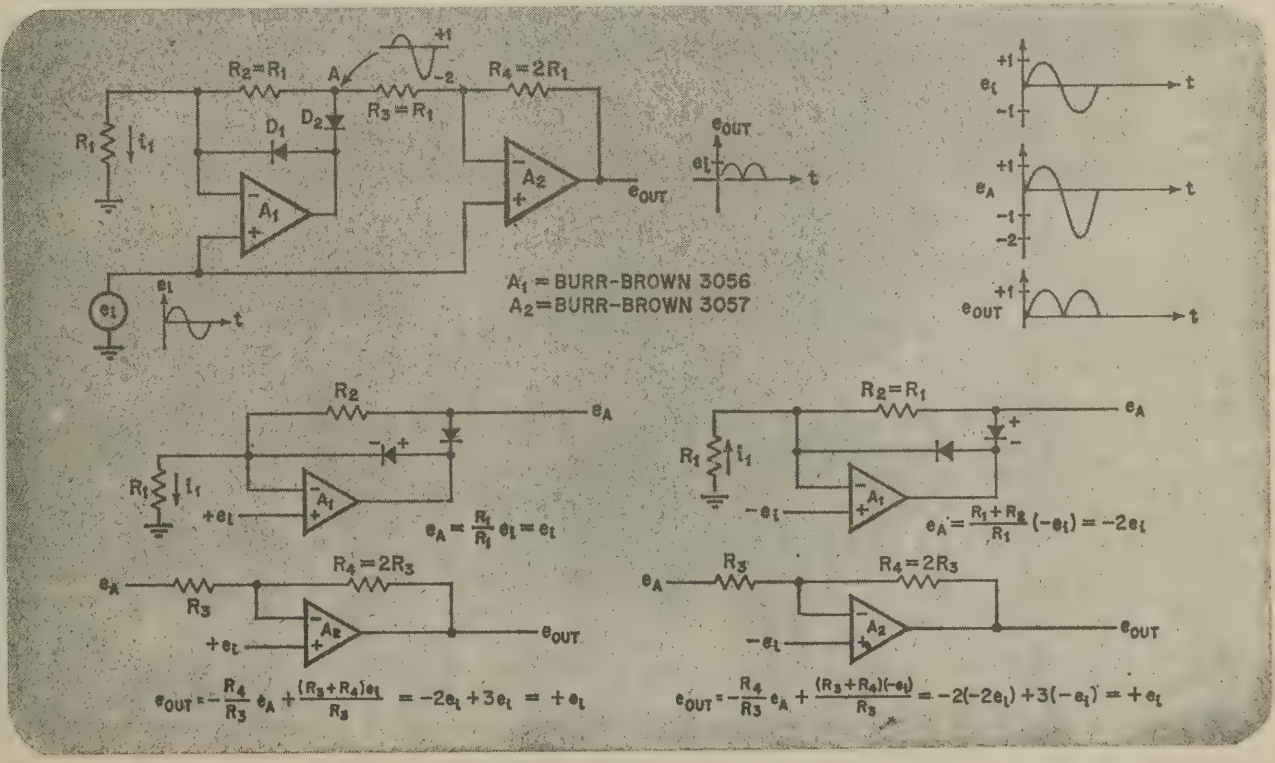
Amplifier A_1 sets up A_2 to complete the rectification process, but not in the same manner as the classic design. Instead of being a half-wave rectifier, A_1 provides a gain of unity if signal e_i is positive and a gain of two if e_i is negative. Then A_2 inverts and doubles the first-stage output giving the input signal a gain of three. Thus, an over-all gain of ± 1 is achieved and a positive output having the absolute value of the signal voltage results.

The partial schematics break down the operation into bite-sized chunks. A_1 develops a positive current i_1 through resistor R_1 with $+e_1$ at the input. The current must go through rectifier D_1 because the amplifier input cannot supply the current and because D_2 is reverse-biased by current of this polarity. Thus forward-biased, D_1 turns on, shorting R_2 out of the feedback path. The gain of A_1 is held to unity, and voltage at node A rises only to $+e_i$.

Conversely, when e_i goes negative, i_1 becomes negative, D_1 turns off and D_2 turns on. Now, the gain goes to 2, and node A goes to $2e_i$.

Stage A2 sums $-2e_i$ and $+3e_i$ at node B, resulting in an output of $+e_i$ regardless of the polarity of the input. The signal-input impedance remains at about 25 MΩ when bipolar-input amplifiers are used and about $10^{11}\Omega$ with FET input op amps. The external resistances have a negligible effect on input characteristics, eliminating the need for a high-impedance input buffer.

Where's the buffer? There is no buffer. Another high-input-impedance op amp is not needed because the signal input always sees a high resistance in the amplifier inputs. The conventional summing resistors are avoided by establishing A_2's output as the sum of $-2e_A$ and $+3e_i$. The output is $(-2e_i + 3e_i)$ or $(+4e_i - 3e_i)$.


$R_2 = R_1$
A
+1
−2
$R_4 = 2R_1$
$R_3 = R_1$
D_1
D_2
R_1
i_1
A_1
A_2
e_{OUT}
e_i
t
A_1 = BURR-BROWN 3056
A_2 = BURR-BROWN 3057
+1
−1
e_A
−2
R_2
$+e_i$
$e_A = \frac{R_1}{R_1} e_i = e_i$
$R_4 = 2R_3$
R_3
$e_{OUT} = -\frac{R_4}{R_3} e_A + \frac{(R_3+R_4)e_i}{R_3} = -2e_i + 3e_i = +e_i$
$-e_i$
$e_A = \frac{R_1+R_2}{R_1}(-e_i) = -2e_i$
$e_{OUT} = -\frac{R_4}{R_3} e_A + \frac{(R_3+R_4)(-e_i)}{R_3} = -2(-2e_i) + 3(-e_i) = +e_i$

Rf linear IC squares high-frequency sine waves

By Norman Tweit and Wes Vincent

Motorola Inc., Scottsdale, Ariz.

Squaring high-frequency sine waves with amplitudes up to about 10 V peak-to-peak is an easy task for low-cost rf linear IC amplifiers. The cascode-connected type of rf/i-f monolithic amplifier needs only an output driver to complete the squaring circuit.

Normally, the automatic gain control function for the IC calls for the differential amplifier to start switching when a control voltage is at a threshold near ground. When the agc voltage on the base of Q_2 increases, Q_2 takes more and more of the emitter current provided by Q_1 and shunts the rf or i-f input signal away from the output transistor, Q_3.

Detecting the zero crossing of a sine wave follows a similar procedure. The sine wave replaces the agc signal, no rf signal is applied to the input stage, and the differential amplifier is biased around ground. In the squaring circuit, the IC substrate is connected to the negative supply voltage.

Q_1 supplies current by switching between Q_2 and Q_3 as the level of the sine wave changes. When the sine wave drops toward zero, Q_3 comes on. The selected value of resistor R_1 allows Q_3 to saturate while biasing off the npn driver transistor, Q_4. The output rises to the supply level of 5 V and remains there until the sine wave comes back up toward zero.

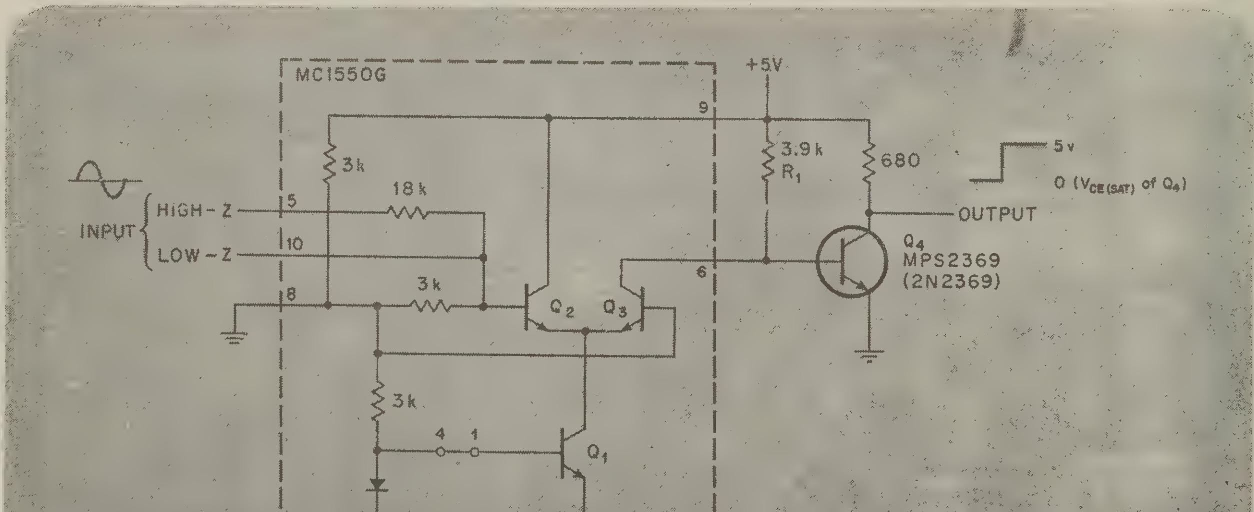
As the input continues rising, Q_2 turns on and Q_3 turns off. When Q_3 is off, its collector is clamped by the base-emitter diode of Q_4, and Q_4 saturates. The output drops to a zero level equal to $V_{CE(sat)}$ of Q_4. The turn-on time for Q_4—about 10 ns—defines the output rise time; the fall time is 25 ns.

The IC supply voltage specifications limit sine-wave amplitudes to a range from about 500 mV peak-to-peak to 10 V pk-pk. Feedthrough at the larger amplitudes—a common problem in Schmitt-trigger types of squaring circuits—doesn't occur. This circuit has an output symmetry of 90% or better to 1 MHz and about 80% at 5 MHz.

The sine wave can be applied to the IC's high-impedance or low-impedance input. The low-Z input gives the best threshold, about 500 mV pk-pk. The 18-kilohm resistor raises the impedance of the low-Z input to form the high-Z input at the cost of reduced threshold.

Together, the IC and the output driver transistor cost about $2.

Round in, square out. Sine-wave control input to Q_1 and Q_3 switches output transistor Q_3 of cascode-connected amplifier on and off. Resistor R_1 makes Q_3 saturate quickly, turning off Q_4 quickly. When Q_3 turns off, Q_4 saturates rapidly. This action gives the output square wave nanosecond rise and fall times, with excellent symmetry.



Stable unijunction VCO needs no critical components

By L. G. Smeins

Ball Brothers Research Corp., Boulder, Colo.

Placing a unijunction transistor and an integrator together produces a voltage-controlled oscillator with more temperature stability than a unijunction VCO and more linearity than an ordinary integrating oscillator.

Unijunction transistor Q_1 serves as a voltage-sensitive reset switch in a Miller integrator formed by amplifier A_1, capacitor C_1 and input resistor R_1. Temperature coefficients are predominantly those of the RC network components, which can be low-drift types. Also, the reset time of Q_1 rather than the output current limit of A_1 determines the linearity of the VCO.

The oscillator's period is

$$t = \frac{C_1(\eta V_{B2} + 0.4)}{I_{in}(1 - \eta)}$$

where η is Q_1's intrinsic standoff ratio, V_{B2} its base-2 voltage and 0.4 its emitter-voltage recovery time (characteristically 0.4 microsecond at C = 0.01 microfarad).

The output of A_1 goes through a peak-to-peak rectifier (D_1, D_2 and C_2, C_3) and a filter (R_2, R_3 and C_3, C_4). Comparator A_2 compares the peak-to-peak value with a reference voltage V_{REF} set by zener diode D_3. The voltage drops through D_1 and D_2 are canceled by D_4 and D_5.

A_2's output drives base 2 of Q_1. Since V_P depends on V_{B2}, the system will seek a level at which the peak-to-peak voltage at the output of A_1 equals V_{REF}. Placing a resistor, R_4, in series with base 2 compensates for the negative coefficient of V_D.

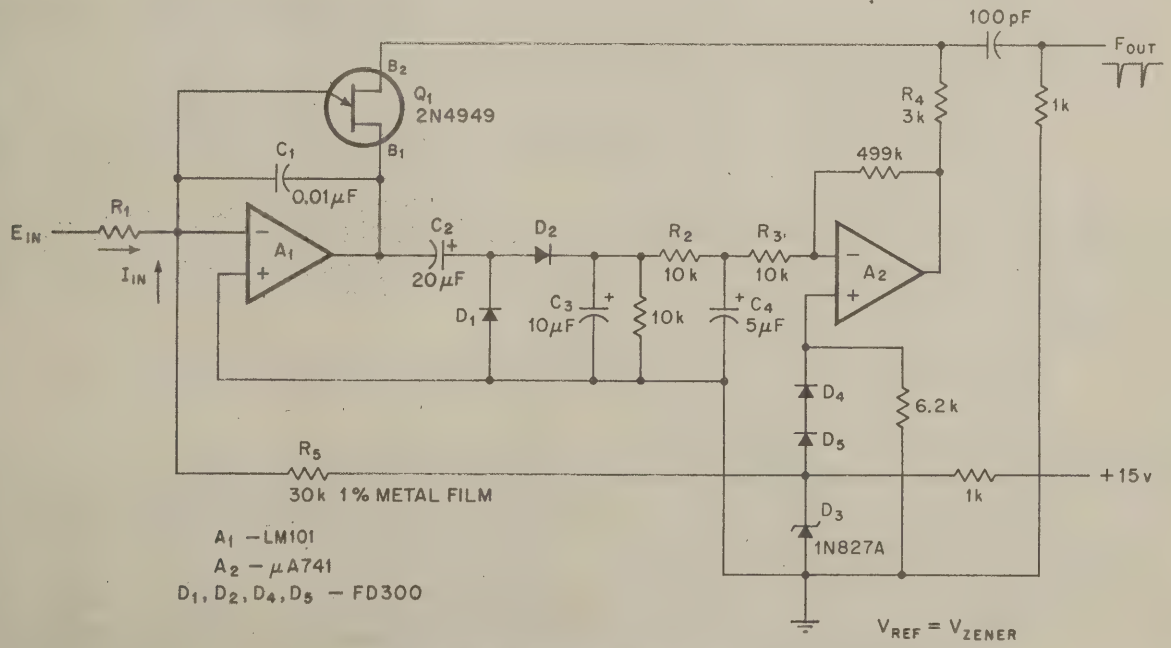
With the closed-loop gain of A_2 now much greater than one and the integrator getting dc feedback through R_5, the oscillation period becomes

$$t = \frac{R_1 R_5 C_1 V_{REF}}{R_5 E_{in} + R_1 V_{REF}}$$

The values shown give a center frequency of approximately 3 kHz, but component values do not have to be specially selected. If C_1 has a temperature coefficient of 100 ppm/°C and the resistors have one of 50 ppm/°C, the VCO coefficient will be about 100 ppm/°C. A voltage follower can drive R_1 if a high input impedance is needed.

Reliable oscillation requires that the current to C_1 be between Q_1's peak-point emitter current I_P and its valley current I_V. In addition, the filter's time constant should be much longer than the period of oscillation, and R_6 should be large enough to allow Q_1 to fire when A_2 is saturated in the positive direction.

All-weather VCO. Temperature coefficients of RC network's passive components limit voltage-controlled oscillator's drift. Unijunction transistor Q_1 is a voltage-sensitive reset switch in integrator A_1. Comparator A_2 stabilizes output, keys period and level to reference voltage.



With some discrete aid IC op amp swings 100 V

By Robert P. Patterson

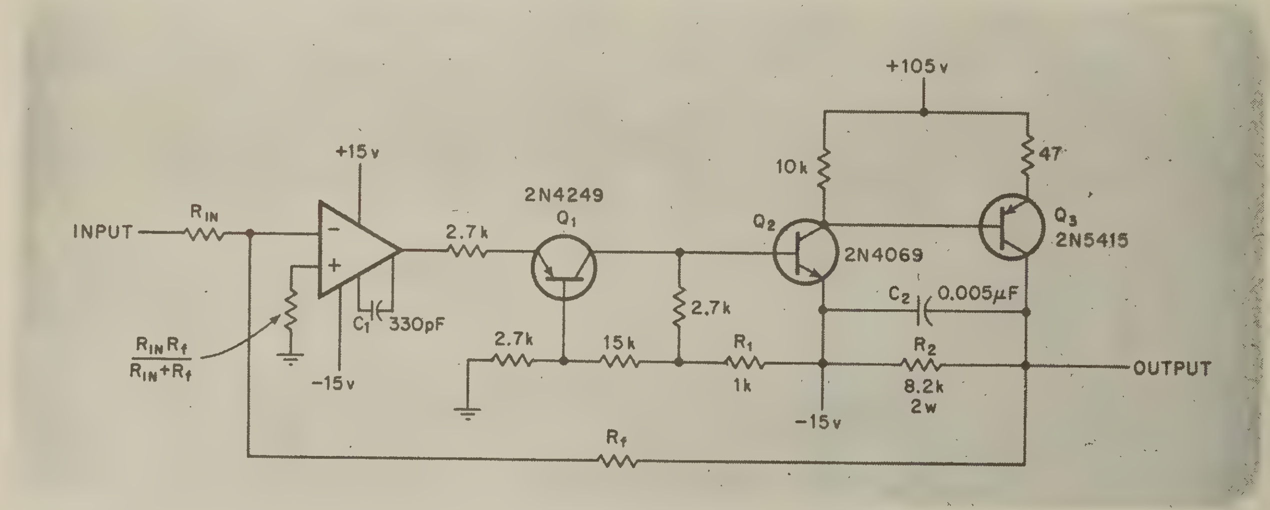
University of Minnesota, Minneapolis

It costs much less to make a hybrid operational amplifier with low-voltage and high-voltage stages than to buy a complete high-voltage op amp. The first stage can be a monolithic op amp.

The design here is a unipolar inverting amplifier with an output swing in closed-loop operation of +100 volts to —10 V. An output between —100 V and +10 V can be obtained by reversing the second-stage supply polarities by making Q_1 and Q_3 npn instead of pnp transistors, and by making Q_2 a pnp type.

Q_1 is a dc level shifter. Q_2 and Q_3 form a direct-coupled amplifier with a gain of about 10, determined by $(R_1 + R_2)/R_1$. With the loop open, approximately —13 V is required at the base of Q_2 for zero output. Capacitor C_2 reduces output noise by rolling off the gain of the discrete transistor stage. Offset and drift are determined by the integrated amplifier.

The IC cannot be an internally compensated op amp. Compensation capacitor C_1 must be much larger than normal (30 pF for the LM101A) to prevent oscillation. The additional open-loop gain of 10 could make the total circuit gain roll-off approach or exceed 12 dB per octave, causing instability.



Low in, high out. Low-voltage monolithic amplifier controls high-voltage discrete amplifier, allowing the output to rise to nearly the high-voltage supply. Output swing of this unipolar inverting amplifier is +100 V to —10 V in closed loop operation.

Feedback limits amplifier better than zeners can

By Paul K. Yee

Zeltex Inc., Concord, Calif.

High gain in a feedback loop of an amplifier limits orders of magnitude more sharply than a conventional zener-diode amplifier limiter, since active limiting is unconstrained by the usual component impedance.

Operational amplifier A_1 operates normally when its output, inverted by A_2, doesn't exceed the limit voltages, $\pm E_L$.

Diodes for amplifiers A_3 and A_4 forestall amplification until the sum voltage at the inverting input of A_1 and A_2 goes above the threshold. Then they amplify open-loop, making their outputs

$$e_3 = -G_3(E_L + e_2) = G_3(E_L + V_{out})$$

for $(E_L - V_{out}) < 0$

$$e_4 = -G_4(-E_L + e_2) = -G_4(-E_L - V_{out})$$

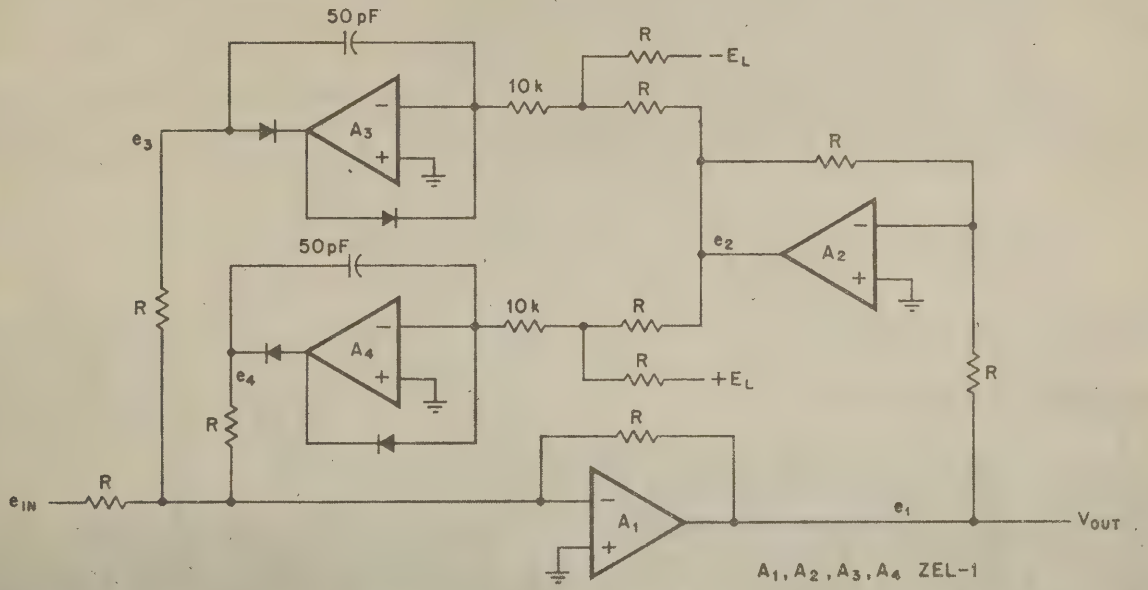
for $(-E_L - V_{out}) > 0$

where G is open-loop gain.

A_1 also inverts; thus, if the output of A_1 drops below $-E_L$, it is driven positive by the added negative feedbacks from A_3, and if it rises above $+E_L$, the positive output of A_4 drives A_1 negatively.

The limiting slope is defined as $\Delta V_{out}/\Delta e_{in}$, or simply the reciprocal of gain in this case. Low-cost amplifiers can provide a slope of 2×10^{-6}.

Loop stability requires that A_3 and A_4 have gain-bandwidth products at least five times lower than those for A_1 and A_2.



Active limiter. Amplifier A_1 quickly drives its output back within limits by generating high-gain feedback through either A_2 and A_3 or A_2 and A_4. The gain-bandwidth product of A_3 and A_4 should be at least five times lower than that for A_1 and A_2 for good loop stability.

Monitor teams spare gates and solid state lamps

By T.F. Prosser

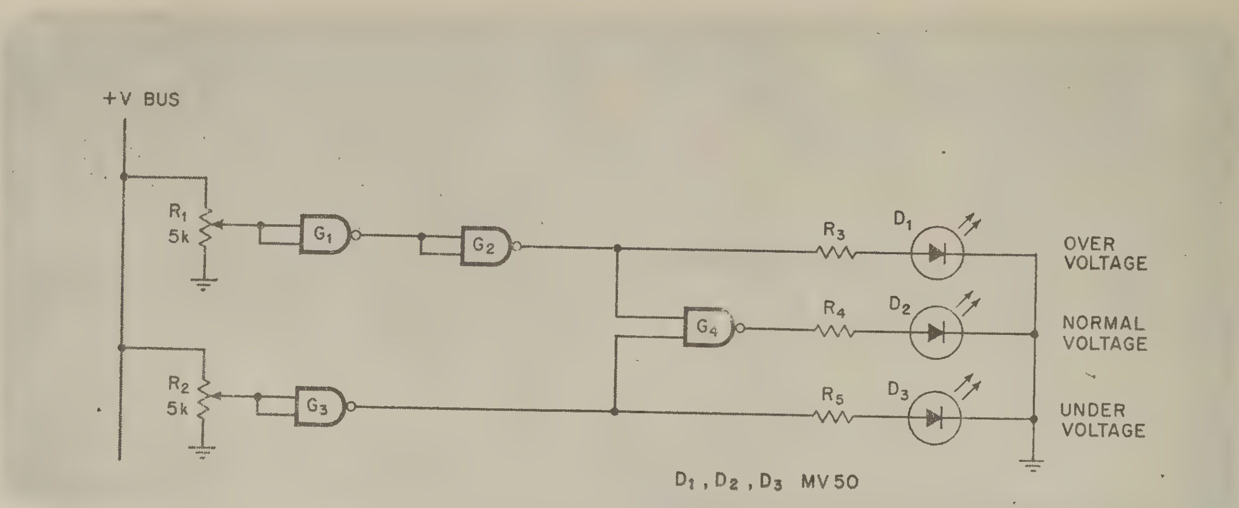
PD Labs, Cupertino, Calif.

Usually, extra gates or inverters are available in IC packages on a logic or power-supply card, and red light-emitting diodes are inexpensive now. Together, they can monitor supply voltages cheaply and reliably.

Variable resistor R_1 is set to switch gate G_1's output from high (logic one) to low (zero) if the positive supply voltage exceeds a maximum such as 5.5 volts for a 5-volt supply. This switches G_2 from low to high and turns on D_1. Conversely, R_2 is set to switch G_3 from low to high and turn on D_3 if the positive voltage drops below a minimum, for example 4.5 volts.

If the voltage is neither too high nor too low, gate G_4 has two low inputs and a high output that keeps D_2 lit. In this normal voltage condition, both D_1 and D_3 are off.

Resistors R_3, R_4, and R_5 limit the logic one output currents of the gates to a value that is safe for the logic family used. Currents as low as 3 milliamperes will light low-cost diodes such as Monsanto Company's MV50.



Condition red. Gates G_1 and G_2 sense an over-voltage on the power-supply line and drive a light-emitting diode D_1 on with a logic "one" output from G_2. If the voltage falls too low, the output of G_3 goes high, and D_3 glows red. Otherwise, only the output of G_4 is high, so only D_3 is lit, when the voltage falls within the limits set by R_1 and R_2.

Op amps find values of buried resistors

By William J. Travis

Sprague World Trade Corp., Ronse (Renaix), Belgium

One resistor in a "T" attenuator or ladder network must be replaced, but which one? The network has been encapsulated and only the terminals can be probed conveniently. Solving three simultaneous equations for each "T" section will identify the resistor—if the measurements or calculations are without errors.

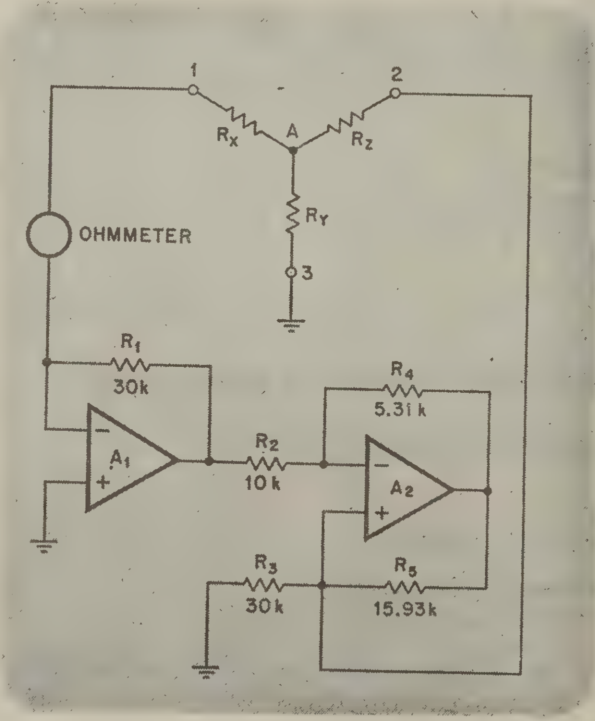
Or, the value of each resistor can be measured directly by connecting the network and meter to a unity-gain current amplifier, A_1 and A_2.

Having the resistors in the "Y" connection guarantees that the current from the ohmmeter entering terminal 1 will be the same as that drawn from terminal 2. Moreover, no current flows in resistor R_y, making the voltage across R_y zero and placing node A at ground potential. Therefore, the meter current can represent only the value of R_x.

By transposing the terminals with a selector switch, R_z and then R_y can be measured.

The ohmmeter reading is accurate for currents up to about 0.3 milliampere for the resistor values shown. The values can be scaled down or up for higher or lower currents. For example, currents to about 3 mA can be measured with R_1 and R_3 at 3 kilohms, R_2 at 1 kΩ, R_4 at 531 ohms, and R_5 at 1.593 kΩ. If desired a multiscale circuit can be prepared on a wafer switch to handle various currents.

Error sources include input bias currents and offset voltages of A_1 and A_2 and common-mode errors of A_2. Field effect transistor inputs will minimize measurement errors.



Measuring R_x. Circuit that measures only the current flow between terminal 1 and node A cures problems of finding value of unknown resistance R_x.

Control voltage resets logic at power turn-on

By Richard L. Wiker

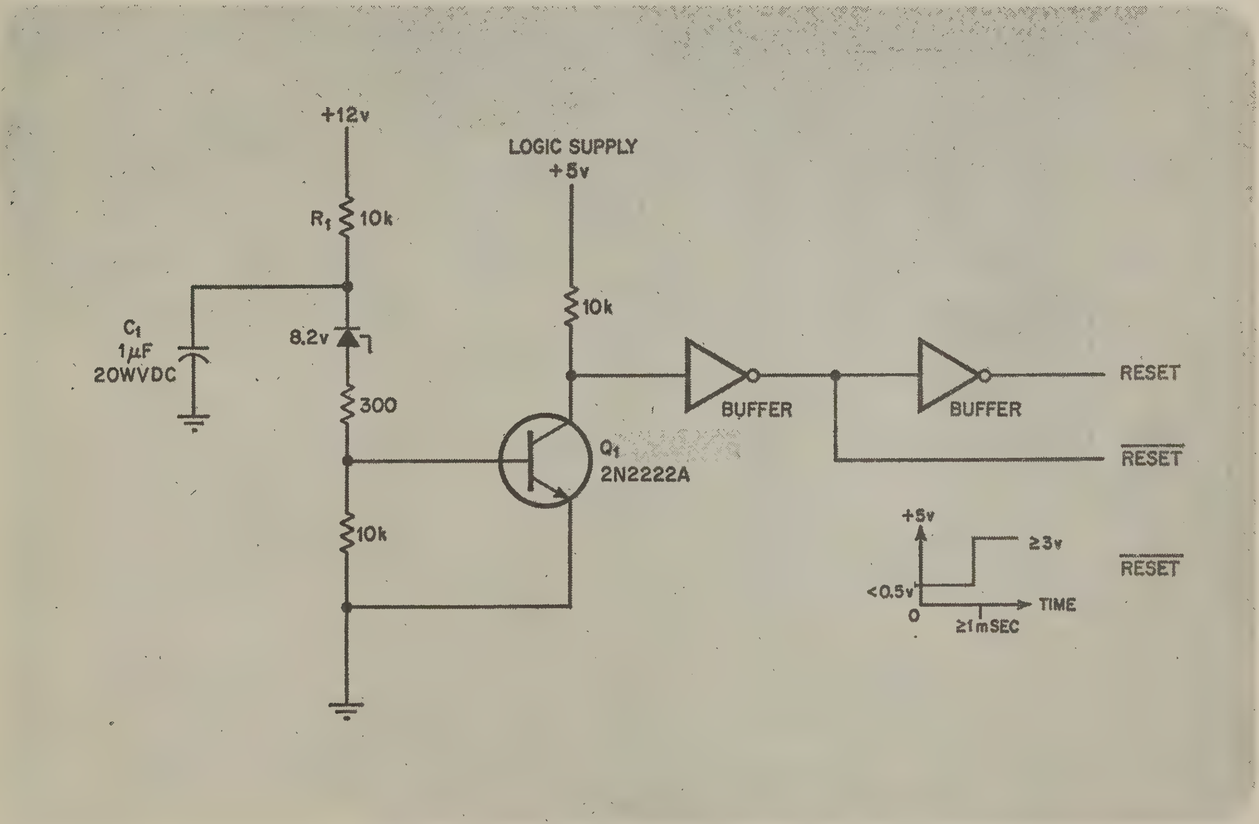
Electronic Communications Inc., St. Petersburg, Fla.

Resetting a logic system at power turn-on takes a pulse of known minimum length. To make sure that the pulse is long enough, regardless of how fast the logic supply rises, another supply voltage in the system can operate a time-delay switch.

As the logic supply rises toward 5 volts, it switches on the first buffer inverter. Then, after a time determined by resistor R_1 and capacitor C_1, the 12 V supply reaches a level that's sufficient to turn on transistor Q_1, which switches the inverter off. The R_1C_1 combination ensures a sufficient delay between the rise of the +5 V logic supply and the turn-on state of the transistor stage to produce at least a 1-millisecond reset pulse.

If the power comes on fast, R_1C_1 mainly determines the pulse width. If the power comes on slowly, the logic supply will reach the logic "1" level well before the 12 V supply exceeds the zener voltage. In either case, after Q_1 turns on, the reset output goes high and stays there. A power interruption long enough to overcome the circuit capacity also causes a reset pulse to be generated.

Both inverters could be eliminated and only a positive reset pulse taken at the collector of Q_1. However, the inverters do sharpen the positive pulse and improve drive. TTL or DTL NAND gates could be used instead of buffer inverters to provide the reset pulses.



Slow turn-on. At power turn-on, the rise in the 5V logic supply generates a reset pulse, and the rise in the 12V supply switches Q_1 and cuts off the pulse. The zener sets the turn-on voltage for Q_1. Using inverters as buffers provides better drive sources to the system logic that's being reset.

Shared one-shot simplifies pulse width converter

By Ken Erickson

Interstate Electronics Corp., Anaheim, Calif.

Most of the one-shots that shorten or stretch pulses in data transfer channels are superfluous. In a digital system many components can be saved by using a single one-shot to control latches that hold the pulse level high for the one-shot's period.

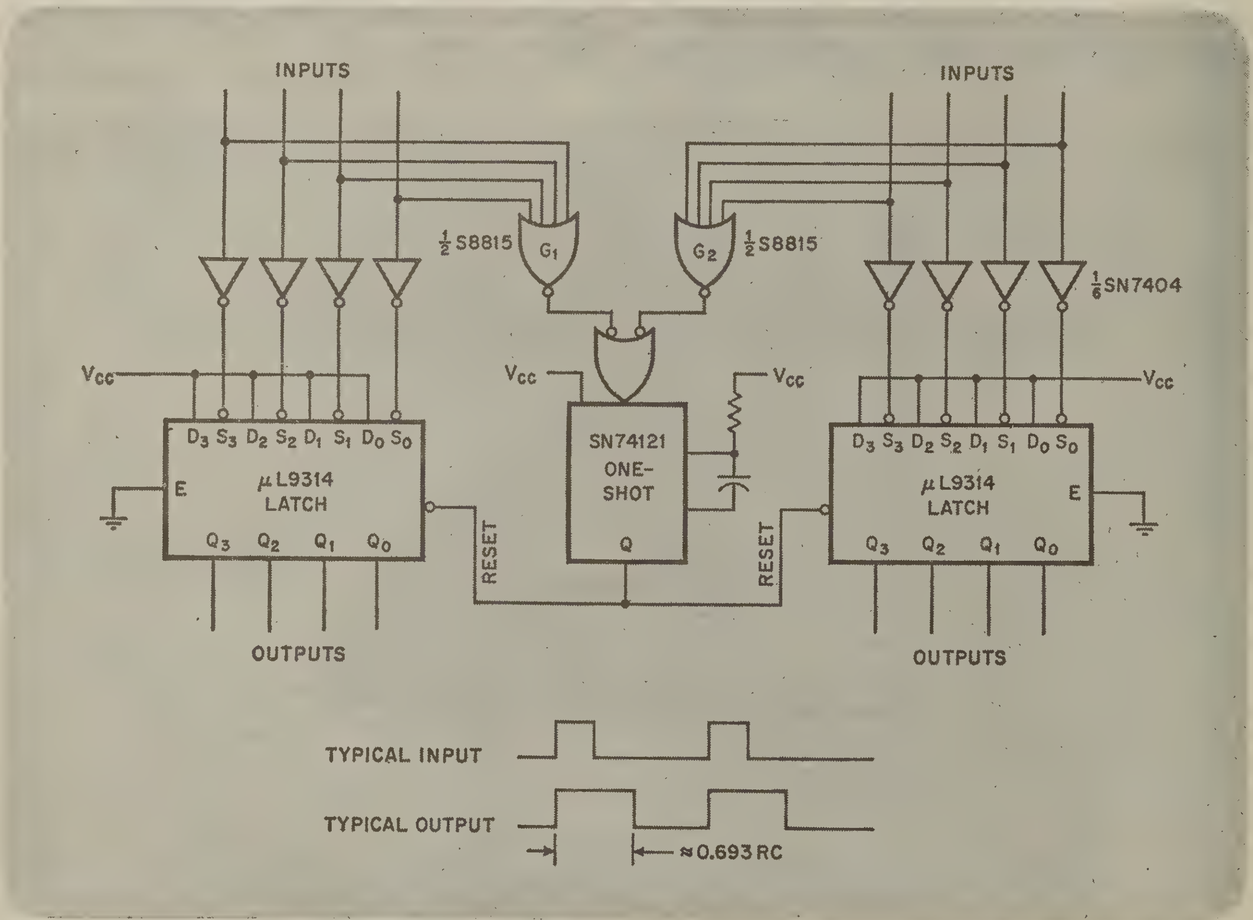
Multichannel pulse width converters can be built with just a four-bit latch for each four channels, a shared one-shot, one resistor, and one capacitor. By contrast, the conventional technique takes three components in each channel—a one-shot and its RC network.

Since the one-shot controls all channels simultaneously, the channels must be synchronous. Buses carrying bit-parallel words or bytes meet this requirement. A typical application is widening pulses to eliminate timing problems when data is clocked into a register.

In the data transfer format, a pulse represents a logical 1 bit and the absence of a pulse a 0 bit. Pulses on any or all input lines switch NOR gate G_1, G_2, or both, to a 0 output, triggering the one-shot, which removes the reset from the latches.

Now the pulses (when inverted) on the input lines enable the set inputs (S_1, etc.) of the latches, causing all to set the corresponding Q outputs to go high. Those outputs remain high until the one-shot times out and restores the reset condition in the latches, dropping the Q outputs. Not including delay in the latches, the output pulse width is about 0.693 RC.

The NOR gates can be omitted if the data bus carries a clock line. The clock is connected to the one-shot so that the triggering clock edge corresponds to the leading edges of the data pulses (the SN74121 has two inputs, one for a negative-going trigger edge and the other for a positive-going one). And the inverters are not needed if the complements of the data pulses are available.



Pulse stretcher. Data pulses on the input lines trigger the one-shot through the NOR gates. The one-shot removes the reset signal from the four-bit latches, allowing the data pulses to set the latch outputs high (V_{cc}). When the one-shot times out, it restores the latch reset condition and the data outputs all return to low.

Diodes prevent power loss and burnout in converters

By Roy Hartkopf

Melbourne, Australia

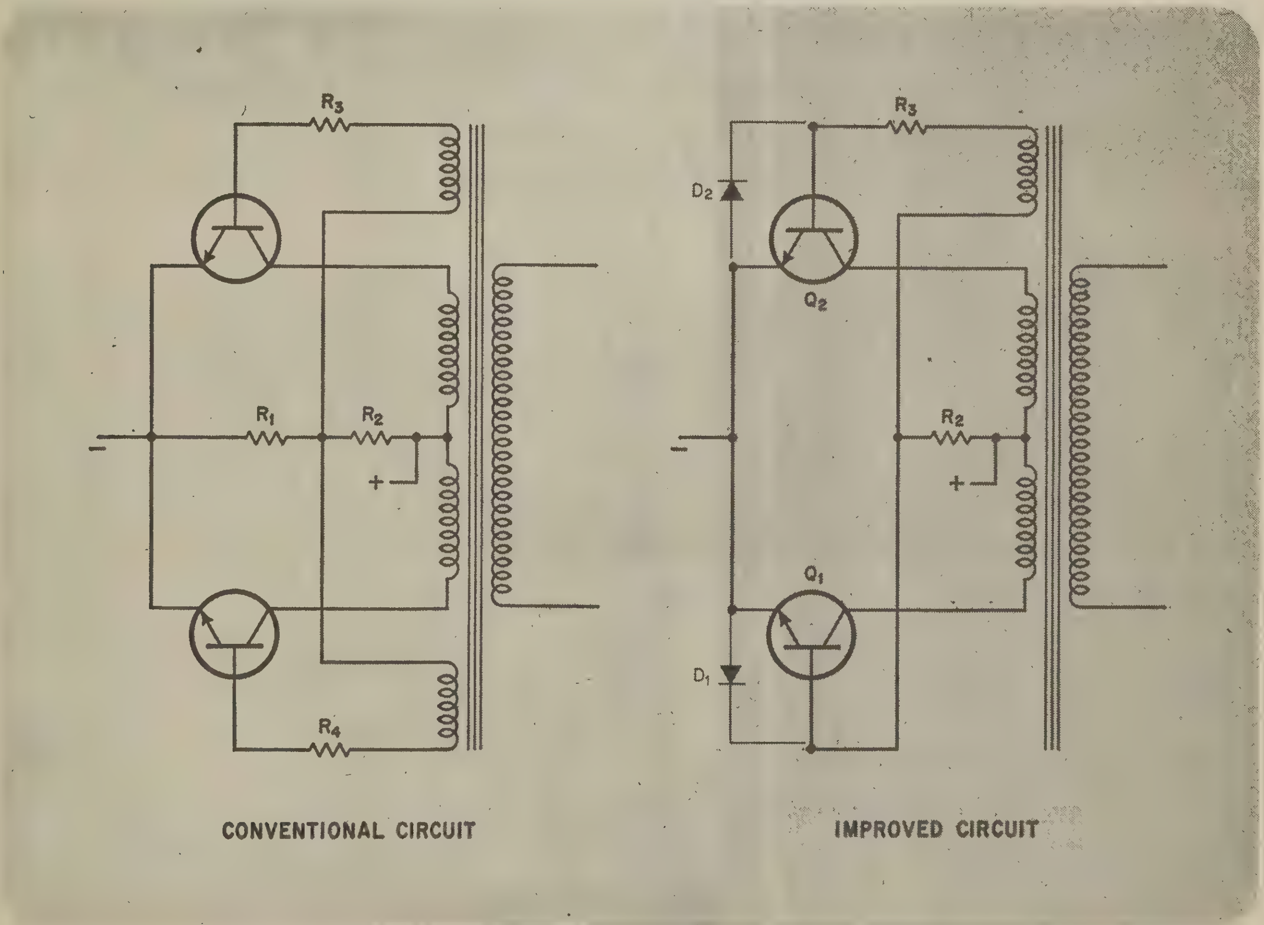
High-power switching transistors in a dc-to-dc converter won't burn out if they're protected by just two low-voltage diodes. Inexpensive silicon power transistors like the 2N3055 with BV_{EBO} ratings of only 5 volts or less can be used with safety. In addition, the new design saves the price of a transformer winding and provides improved performance.

In the conventional circuit, the reverse base-emitter voltage of the transistor that is cut off can easily exceed breakdown levels. The bias winding that supplies the transistor is unloaded and undamped, and its voltage is in series with the reverse voltage that's developed across resistor R_1 by the base current of the saturated transistor.

At best, the design is inefficient. R_1 and R_2 provide the starting forward bias. The resistance of R_1 should be large for good starting with minimum current, yet should be small to minimize any voltage drop across it caused by the peak base-emitter current of the saturated transistor. The compromise results in wasted power. The base current is limited by adjusting R_3 and R_4.

But in the improved design, diodes D_1 and D_2 limit the reverse bias across the cutoff transistor to the forward voltage drop of the diodes on that side, usually about 1 volt. With the single bias winding loaded evenly on both halves of the cycle no transients are developed. Operation is symmetrical because the bias winding and R_3 are in series with each base alternately. And the need for R_1, with all its conflicting requirements, is eliminated.

The circuit starts easier and wastes little power. Starting bias favors Q_1 since R_3 is in the series with the base of Q_2 at startup. Also, with R_1 eliminated, only a few milliamps of bias current need flow to the transistors. Both resistors can be adjusted to increase power output and efficiency.



CONVENTIONAL CIRCUIT

IMPROVED CIRCUIT

Quick change. Converter's old-style chopper circuit is updated by adding two diodes with PIVs of 50 volts, snipping out resistor R_1 and using only one bias winding. The diodes prevent breakdown of the transistor base-emitter junction during reverse bias and elimination of R_1 reduces the needed transistor bias current.

Fail-safe flame sensor provides control functions

By Russell Wolfram

Stanford Research Institute, Menlo Park, Calif.

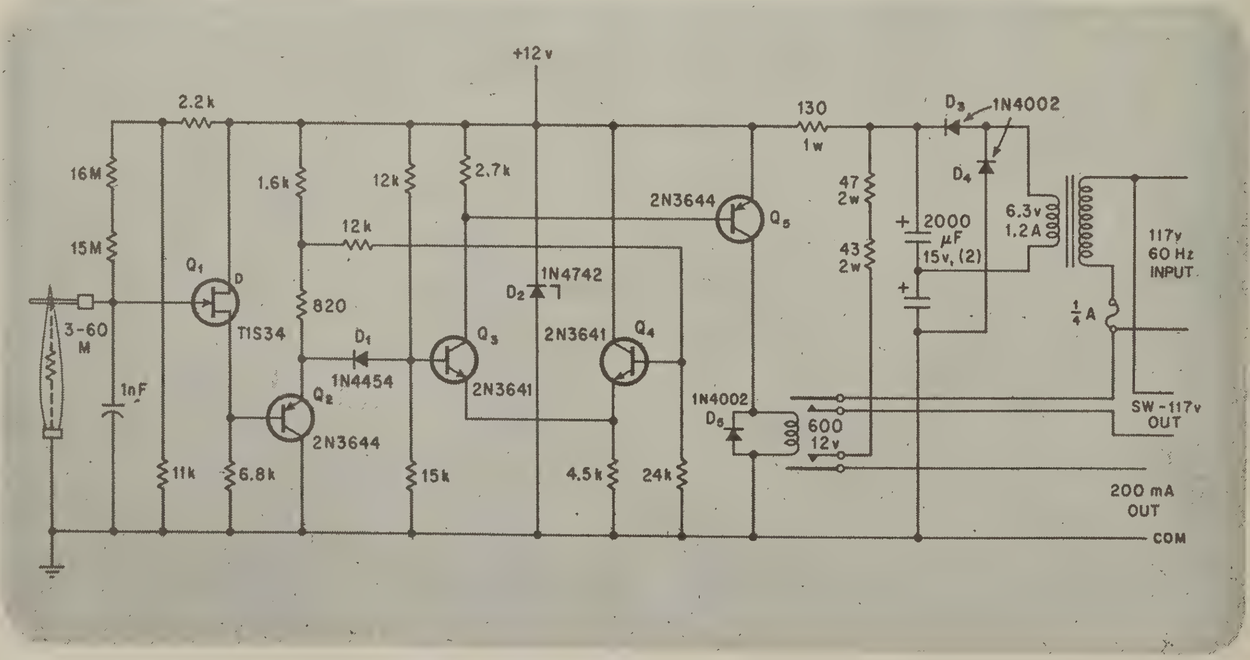
An electronic flame sensor is mandatory for monitoring and control applications where high temperature, excessive ambient light or response time requirements preclude the use of thermocouples or photocells.

This circuit operates over a range of flame resistances from 30 to 60 megohms. It provides both a relay-operated, 200-milliampere current supply for controlling a low-resistance electric gas valve, and a convenient contact closure for other control functions. The circuit is returned to the off condition either by loss of flame or by grounding of the sensing rod.

The flame resistance forms part of a high-resistance voltage divider which drives the source follower impedance transformer, Q_1. This in turn feeds pnp emitter follower Q_2. The tapped emitter resistor of this stage provides both the usual emitter voltage and a positive offset voltage output. This voltage is coupled through a voltage divider to one input of a differential amplifier. The emitter voltage is diode-coupled to the other amplifier input. Differential amplifier Q_3-Q_4 is biased so that, with a flame resistance within the operating range, Q_3 and Q_5 conduct and the relay is energized.

If the flame is extinguished, the emitter voltage of Q_2 rises nearly to the supply voltage. Coupling diode D_1 is reverse-biased which leaves Q_3 unaffected but pulls up the base of Q_4. By conducting, Q_4 turns off Q_3, Q_5, and the relay. If the sensor rod is short-circuited to ground, the emitter of Q_2 drops to a lower voltage, pulling the base of Q_3 down with it through D_1. The base voltage of Q_4 is also pulled down, but by a lesser amount because of the voltage-divider coupling network. The result is that Q_4 conducts, again turning off Q_3, Q_5, and the relay.

For the flame-out condition, the circuit is fail-safe for all active components except Q_4. For the power supply, a zener-regulated voltage doubler utilizes a standard 6.3-volt filament transformer.



Fail-safe. All-electronic sensor uses no thermocouples or photocells to detect flame-out. Relay remains energized as long as flame is burning. Should flame be extinguished or if the sensor rod is grounded, Q_4 conducts, turning off Q_3 and relay driver Q_5.

Single hex inverter picks data signals from noise

By Charles A. Herbst

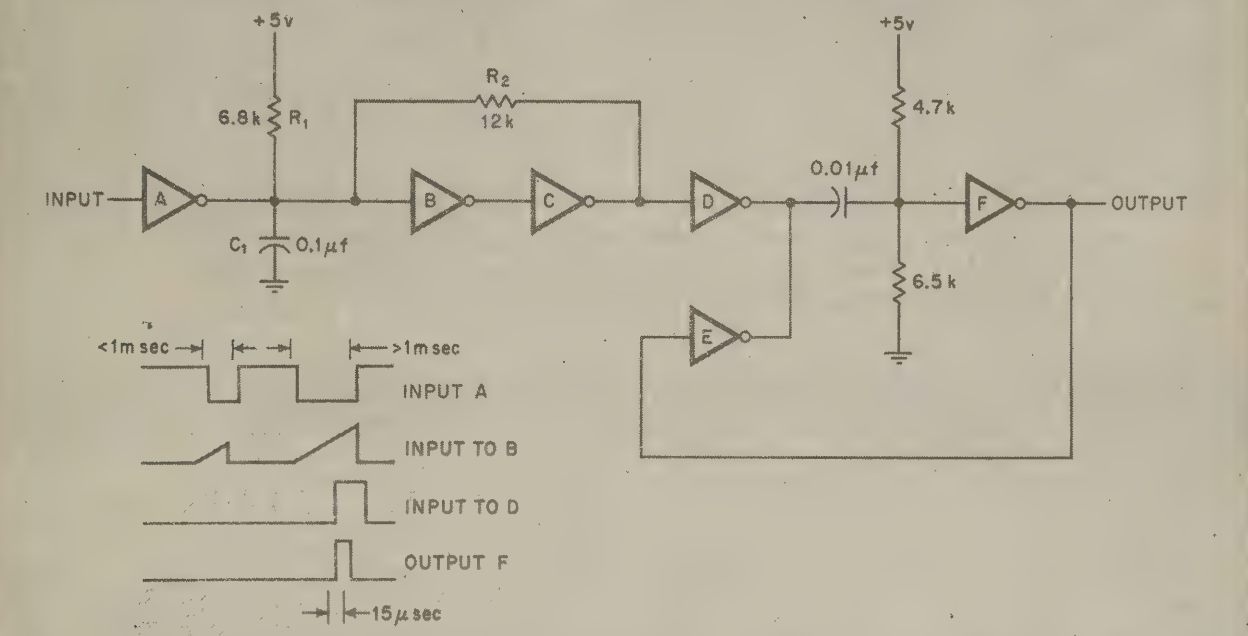
Dumont, N.J.

Noise spikes can be eliminated from a digital tape-recording or signal-processing channel with just a single package of diode-transistor logic and a few timing components. The DTL hex inverter, which functions as a pulse width discriminator and pulse generator, decides if the incoming pulses are too narrow to be data bits. Those that qualify as data bits finally produce fixed-width pulses.

Capacitor C_1 is normally in a discharged condition at the output of inverter A. The negative-going edge of an input pulse causes C_1 to begin charging toward 5 volts. If the pulse is long enough for C_1 to charge up to about 1.5 volts, through R_1, inverter B will switch and cause the output of inverter C to go positive. Positive feedback through R_2 insures a rapid change of state.

Now, the positive input to inverter D makes the monostable multivibrator—inverters E and F—generate an output pulse whose width is fixed by the time constant of the RC network. But if the original input pulse is too short, there is no output pulse. Capacitor C_1 is again discharged.

The component values allow the input stage to sense pulses longer than 1 ms and the output stage to generate pulses about 15 μs wide.



Discrimination. The monostable multivibrator can't be triggered unless the input inverter sees a pulse long enough to charge C_1 to 1.5 volts. This voltage level triggers inverters B, C, and D, making the one-shot generate a pulse. Short noise spikes never get past inverter A.

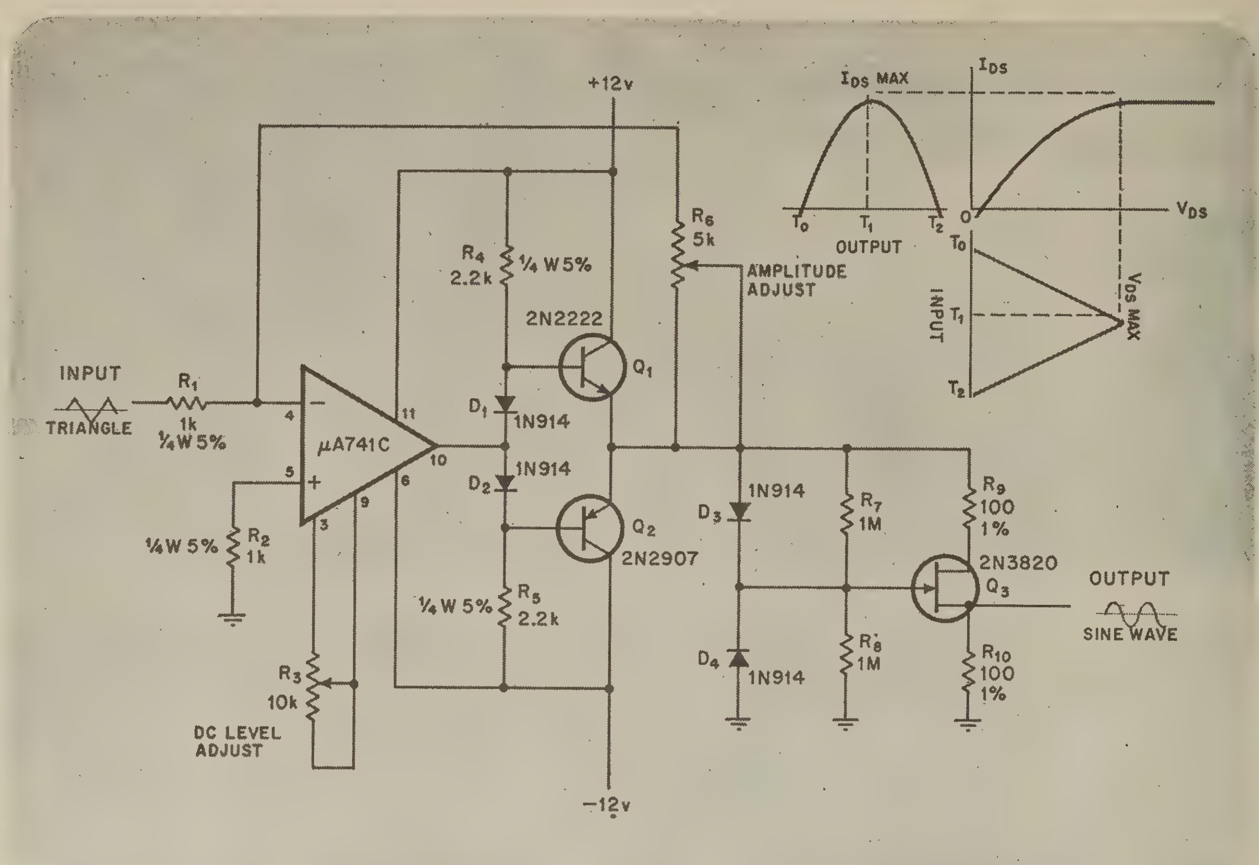
Field effect transistor converts triangles to sines

By William E. Peterson

ITL Research Corp., Northridge, California

Conversion of triangular waveshapes to sinusoids is usually accomplished by diode-resistor shaping networks, which reconstruct the sine wave segment by segment. A much simpler method exploits an unusual property of junction field effect transistors.[1]

The principle is illustrated in the figure. A triangular-shaped voltage is applied across the drain and source of a junction FET with its gate



Easy conversion. Transfer characteristic of junction field effect transistor resembles a sinusoid, providing mechanism for triangle-to-sine conversion. In circuit, monolithic op amp provides gain for driving junction FET Q_3. Two simple control adjustments yield sinusoid with less than 2% distortion.

lead grounded. The drain-source channel has a low impedance, and the triangular wave source must be capable of delivering adequate current.

The FET transfer curve in the region below V_{DS} closely approximates a quarter sinusoid. If the triangle amplitude is carefully adjusted so that its peak corresponds to V_{DSmax}, the current I_{DS} flowing through the channel takes the form of a segment of a sinusoid. This scheme produces the first half of the sine wave. The other half is generated by the reciprocal characteristics of the drain and source leads. That is, as long as gate polarity is preserved, the drain and source may be interchanged to produce a mirror image of the FET transfer curve across the I_{DS} axis. Thus, a negative triangular input varying about ground will yield a sinusoidal drain-source current of opposite polarity.

A practical implementation of the converter is shown in the schematic. An operational amplifier (μA741C) provides the necessary gain with the addition of low-impedance drive network Q_1-Q_2. Fairchild epoxy FET Q_3 furnishes the desired transfer characteristic. Potentiometer R_6 sets the triangle amplitude. Resistors R_9 and R_{10} provide degenerative feedback to reduce harmonic distortion of the sinewave output. Diodes D_3 and D_4 provide the necessary switching of the gate lead during the crossover of the signal polarity.

Harmonic distortion of less than 2% is easily achieved with the two controls and a CRT. For proper operation, the input triangle waveform must have constant peak-to-peak amplitude, swinging about ground. To adjust the converter with a given triangle amplitude, control R_6 is varied while the output is viewed on a CRT until the peaks of the output waveform are just beginning to round off. Next, the d-c level control R_3 is varied to adjust the positive and negative portions of the sinusoid for symmetry, while the final triangle amplitude is achieved with R_6.

Since the circuit operates as a nonreactive filter the input frequency is restricted only by the operational amplifier's rolloff frequency of 10 kHz. Higher frequency operation may be achieved with a different operational amplifier.

Reference

1. R.D. Middlebrook and I. Richer, "Nonreactive filter converts triangular waves to sines," **Electronics, March 8, 1965, p. 96.**

Flashlight helps monitor voltage levels

By Ralph S. Granchelli,

Framingham, Mass.

A flashlight can illuminate the problems of monitoring and adjusting power supplies with outputs that are inaccessible or dangerous to probe. The light beam turns on photocells whose resistance then changes, activating lamps indicating whether the supply voltage is within preset limits.

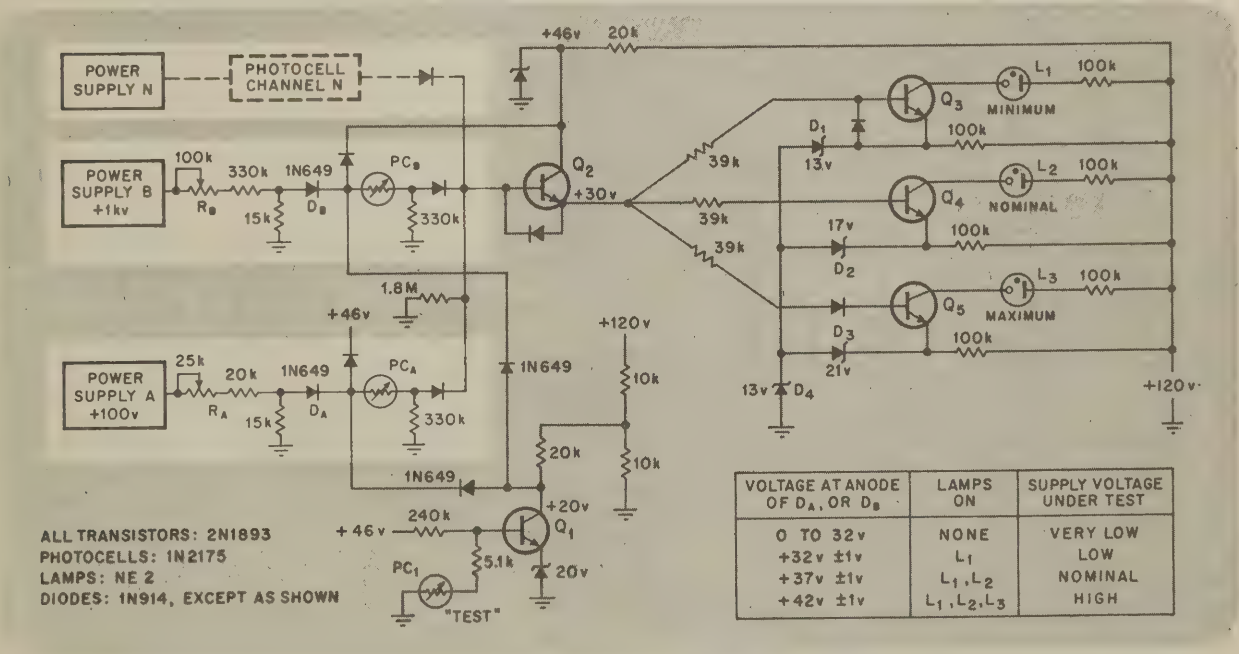
A large number of supplies can share the same indicators. Each monitoring channel contains a photocell, a variable voltage divider network to obtain the test voltages, and diodes to establish levels.

The indicator lamp circuits are tested by illuminating photocell PC_1, which cuts off transistor Q_1, driving photocells PC_A, PC_B and PC_N to a 46.5-volt clamp level. When any of the photocells is illuminated, all the lamps should light, then go out when the illuminating beam is removed.

Illuminating any one of the photocells reduces its cell resistance. Thus Q_2 can turn on Q_3, Q_4, and Q_5, depending on the voltage at the anode of D_A, D_B, and D_N. Each voltage divider's output is adjusted for 37 volts ±1 volt, sufficient to turn on Q_2 when the power supply voltage is at the nominal value. If so, lamps L_1 and L_2 will light. If it's low, but within 15% of the nominal setting, only L_1 will light; if too high by 15%, all the lamps will light. An adjustable supply then can be corrected in the right direction until nominal conditions are indicated. Furthermore, any tolerance can be set up by selecting the proper zener voltages.

When the photocells are not illuminated, the lamps are off because the emitter of Q_2 is held at 30 volts by zener diodes D_1 and D_4. Transistors Q_3, Q_4, and Q_5, are reverse-biased at this time. The four zeners act as comparator references.

Ambient light will not switch on the photocells, so they can be located behind a glass port in the power supply housing. Remote cells can be reached through light pipes or other light directors. The rheostats can be oil-sealed, if necessary, or replaced by fixed resistors in the housing.



ALL TRANSISTORS: 2N1893
PHOTOCELLS: 1N2175
LAMPS: NE 2
DIODES: 1N914, EXCEPT AS SHOWN

VOLTAGE AT ANODE OF D_A, OR D_B	LAMPS ON	SUPPLY VOLTAGE UNDER TEST
0 TO 32v	NONE	VERY LOW
+32v ±1v	L_1	LOW
+37v ±1v	L_1, L_2	NOMINAL
+42v ±1v	L_1, L_2, L_3	HIGH

High-voltage peephole. One or more of the indicator lamps will light if the supply voltage is within ± 15% of its nominal value. The channel to be monitored is selected by illuminating a photocell; the indicator lamps light according to whether the power supply voltage is above, below, or at the nominal voltage.

Low-cost digital ICs prevent operator errors

By Ivars P. Breikss,

Test Instrument division, Honeywell Inc., Denver, Colo.

With many companies employing relatively unskilled people to run electronic equipment, designers must make sure that controls cannot be set to conflicting modes of operation that would damage sensitive gear.

Backing up the control switches with mutually exclusive logic is one effective approach. The logic need not be elaborate. Only five diode-transistor logic packages can control four functions. The lamps indicate operating modes and stop all functions, regardless of switch positions, after power is interrupted.

The NAND gates are connected as four set-reset binaries. Each binary is set by a momentary closure of the corresponding switch.

Suppose switch S_1 closes. Output A rises to about 5 volts (logic 1) and, when inverted, resets the other binaries to B, C, and D outputs of 0 volt (logic 0). The complementary "stop" function $\overline{A}$ will also be disabled and $\overline{B}$, $\overline{C}$, and $\overline{D}$ enabled—the other outputs go to their open-switch states.

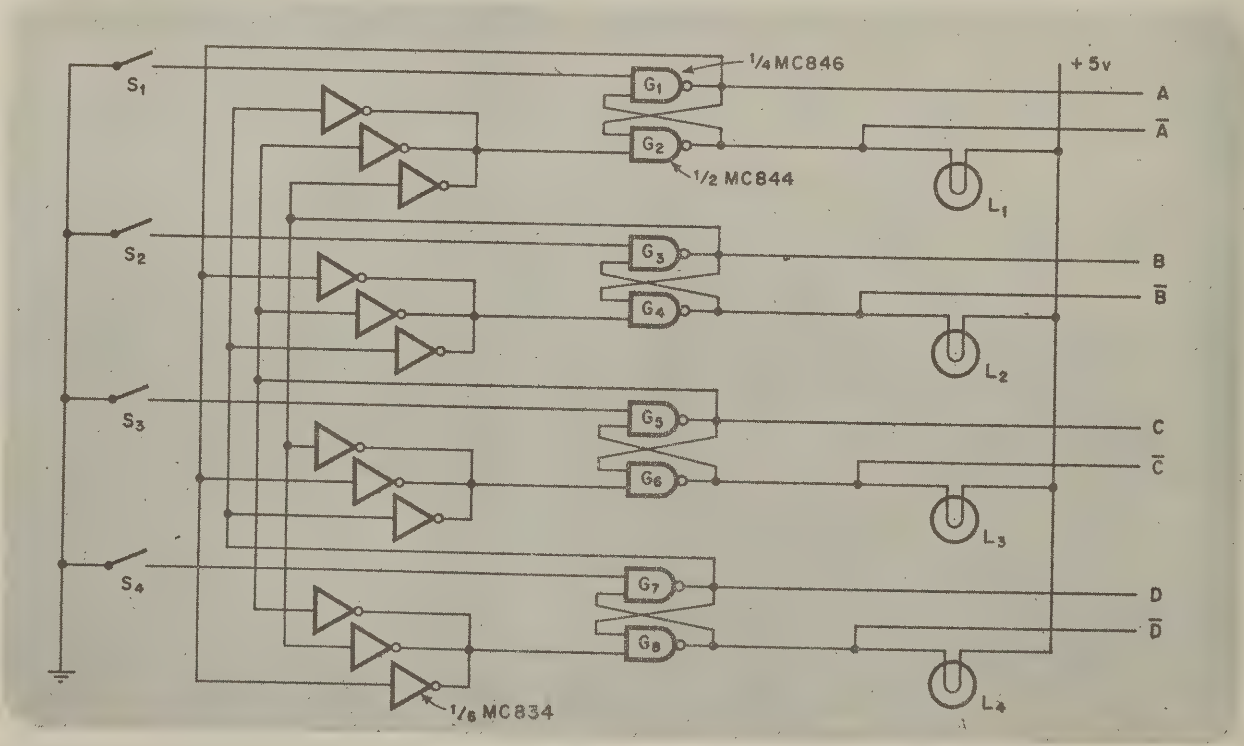
The incandescent lamps indicate the equipment operating mode. Lamp L_1 lights because it is between 5 volts and $\overline{A} = 0$ volt. Little or no potential is across the other lamps, and they remain unlit.

If two or more switches are closed simultaneously, all uncomplemented outputs go low and all complemented outputs go high. And if several switches are closed sequentially, only the last switch will enable its function and light its lamp.

The difference between the hot and cold resistances of a lamp forces all outputs to a predictable state—all stop—when power is turned on or restored after an interruption. The low resistances of the cold filaments cause the $\overline{A}$, $\overline{B}$, $\overline{C}$ and $\overline{D}$ outputs to rise to 5 volts. The next switch closure then resets the binaries.

Gates G_2, G_4, G_6, and G_8 have to take a lamp turn-on surge. The MC844 power gates can sink 100 milliamperes and limit any higher current with their output transistors. Substituting inverters for G_1, G_3, G_5 and G_7 will eliminate the voltage drop across the power gates and brighten the lamps. However, the circuit will not disable all functions if two switches are closed at the same time.

More switch positions can be added within the fanout and wired-OR limitations of the logic types used. The DTL inverters can be replaced by transistor-transistor logic with wired-OR capability and open-collector outputs, or with NOR gates.



Safety first. No control conflicts here. Only one switch closure at a time is honored by the binaries; the lamps cancel previous settings at turn-on. Closing of more than one of the switches simultaneously causes all the outputs to assume the zero state.

Comparator and multivibrator add up to a linear VCO

By Eric Breeze,

Fairchild Semiconductor division, Mountain View, Calif.

A pulse period that ranges widely but linearly with control voltage, and provides correct timing between the first and last pulses, can allow a voltage-controlled oscillator to double as an analog-to-digital converter, or even a digital voltmeter.

This can be effected by retriggering a one-shot multivibrator with a comparator. Standard logic levels start and stop the one-shot multivibrator; the control input level setting determines when the comparator retriggers the one-shot to start the next cycle. The pulse period depends on the time it takes for the linear ramp discharge to reach the level at which the control input voltage was set.

When the keying input voltage is raised from 0 to 5 volts (logical 0 to1) the one-shot is triggered and generates the first output pulse. If the keying input is held at this level, the one-shot remains enabled, so it can be retriggered through its NOR gate input.

The one-shot's complementary output causes transistor Q_1 to conduct, providing a path for capacitor C_1 to charge to +5 volts. After the one-shot times out, Q_1 turns off and C_1 starts to discharge through the constant-current path formed by Q_2 and R_1. Therefore, the voltage at point A is a ramp function that is linear with respect to time between +5 volts and about −6 volts.

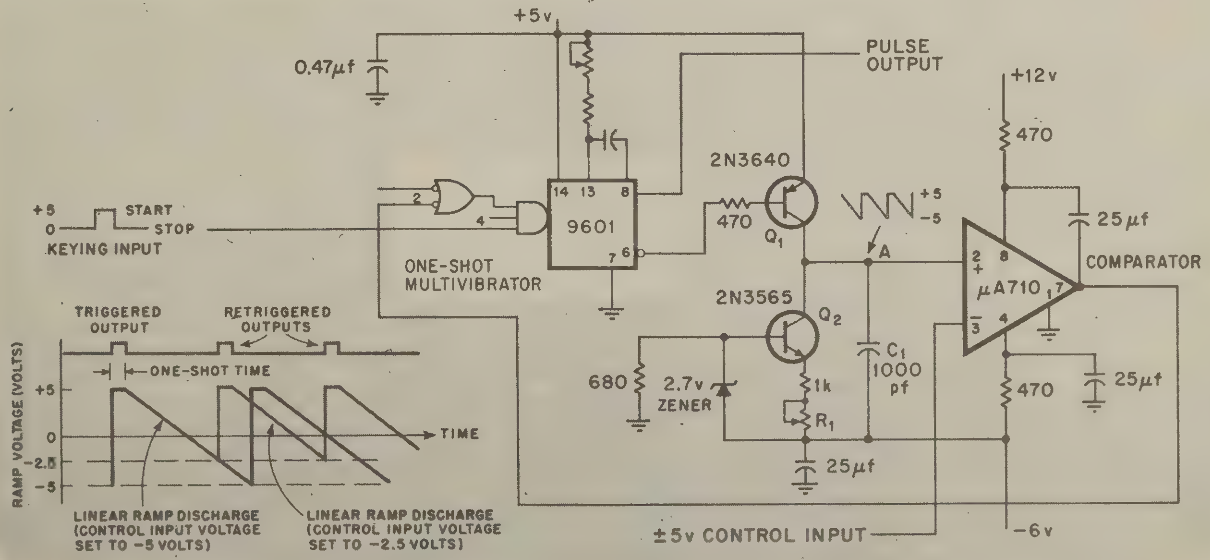
As soon as the ramp voltage reaches the control voltage level on the comparator's inverting input, the comparator's output goes high, retriggering the one-shot, and the next output pulse is generated. The higher the control input voltage, the shorter the output pulse period.

R_1 should be adjusted to linearize the ramp voltage between +5 and −5 volts at the lowest oscillator frequency desired, that is, to adjust the ramp slope. For a control input voltage of ±5 volts it's possible to achieve a 40:1 range—50 kilohertz to 2 megahertz—with the components shown. The leads must be kept very short when operating in the megahertz region.

Operation at lower frequencies, down to 1 hz, can be achieved by increasing C_1 and by lengthening the one-shot pulse width. A 20-picofarad one-shot timing capacitor yields a pulse of about 150 nanoseconds but the capacitor can be much larger.

Maximum frequency is limited by the one-shot time. The 9601's maximum repetition rate is above 10 Mhz, compatible with the μA710's response time of about 40 nsec.

Oscillation is stopped by dropping the keying input to zero. Therefore, a short keying pulse will generate only a single comparator output, making the circuit a voltage-variable time delay. The value of an unknown control voltage also can be found digitally by clocking the time between the falling edge of the one-shot output and the leading edge of the comparator output. Or the keying input level can be held high and the output used for control and display functions.



Multifrequency multivibrator. When the keying input goes high, the one-shot multivibrator generates a pulse that lets C_1 charge to + 5 volts through Q_1. After the one-shot times out, C_1 discharges linearly through Q_2 and R_1 until the voltage at the positive terminal of the comparator equals the control input voltage at the negative terminal.

Storage coil cuts relay pull-in delay

By Joseph Gaon

JMR Electronics Corp., Bronx, N.Y.

Energy stored in a nearby coil will eliminate the electrical delay in the pull-in time of a magnetic relay or solenoid. The circuit operates an industrial control relay in only 5 milliseconds—the mechanical reaction time—compared with the normal 16 msec.

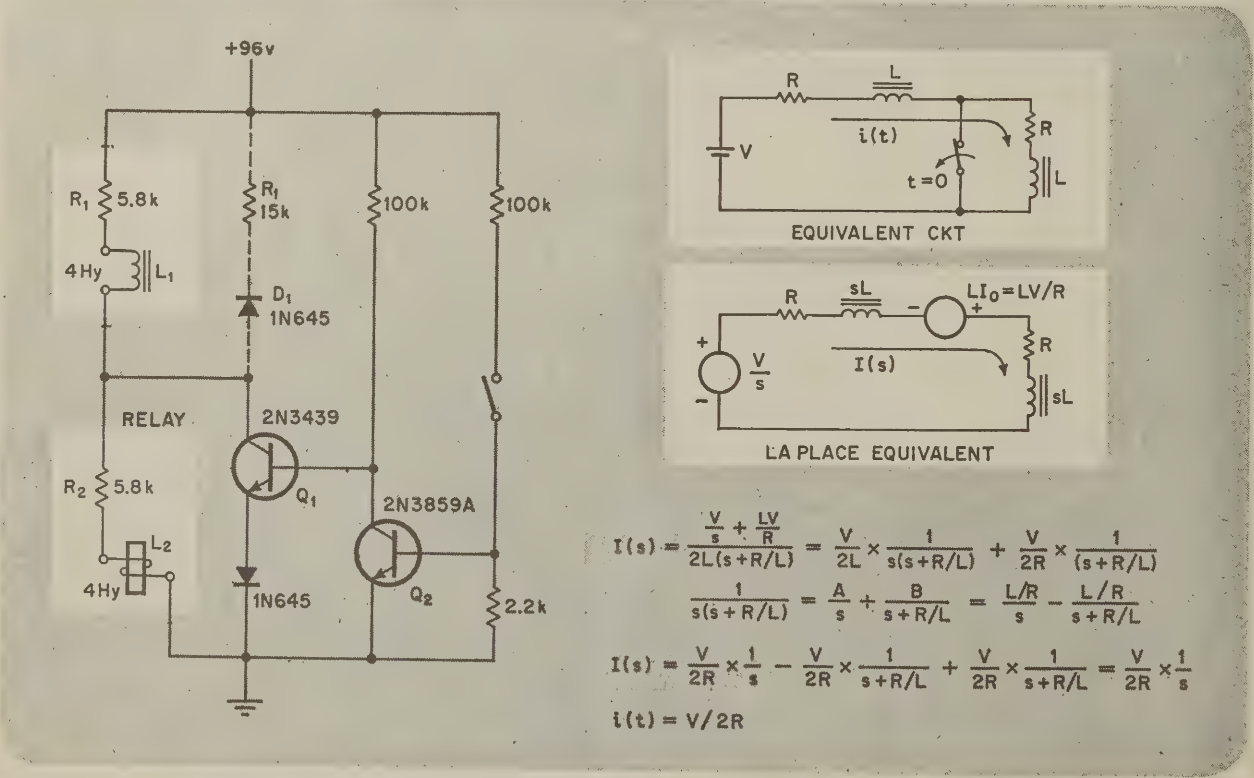
Opening the switch short circuits the relay. In this steady-state condition, transistor Q_1 is off, Q_2 is on, and current flows through inductor I_1.

Closing the switch turns Q_2 off and Q_1 on, causing the field in the inductor to collapse. The inductor generates a large voltage spike that is integrated by the relay, L_2-R_2. The current in the relay is a stop function rather than an exponential buildup, as proven by the analysis of the equivalent circuit. So there is no electrical delay time required to build up the current through the relay coil.

Also, it can be seen that the applied voltage, 96 volts in this example, must be twice the nominal voltage of the relay. The inductor and the relay must have equal resistances and inductances, within normal tolerances.

Since the brunt is borne by the inductor, a relay identical to the operating relay may be used for I_1 and R_1, if it can withstand twice the nominal coil voltage. The dummy relay's armature is jammed open so that L_1 will equal L_2 when the armature of the operating relay is unseated.

Optional diode D_1 and resistor R_3 may be added to guard against a collector-to-emitter breakdown of Q_1. However, adding the devices will cause a slight electrical delay.



$$I(s) = \frac{\frac{V}{s} + \frac{LV}{R}}{2L(s+R/L)} = \frac{V}{2L} \times \frac{1}{s(s+R/L)} + \frac{V}{2R} \times \frac{1}{(s+R/L)}$$

$$\frac{1}{s(s+R/L)} = \frac{A}{s} + \frac{B}{s+R/L} = \frac{L/R}{s} - \frac{L/R}{s+R/L}$$

$$I(s) = \frac{V}{2R} \times \frac{1}{s} - \frac{V}{2R} \times \frac{1}{s+R/L} + \frac{V}{2R} \times \frac{1}{s+R/L} = \frac{V}{2R} \times \frac{1}{s}$$

$$i(t) = V/2R$$

Big but fast. Industrial control circuit gets set for fast relay operation by routing steady-state current through inductor L_1 when relay is short-circuted by the switch. Closing the switch collapses the inductor field. The voltage impulse is rapidly integrated by the relay as a current step, eliminating the normal electrical delay.

Wave squarer shifts phase as much as 360°

By Walter G. Jung

Forest Hill, Md.

A sine-wave to square-wave converter that's half linear and half digital produces pulse trains shifted in phase as much as 360° from the analog input. The circuit can't be saturated or overdriven, and the outputs remain at the integrated circuit logic levels of zero to 5 volts over a wide range of analog-signal amplitudes.

The input stage—a radio-frequency and intermediate-frequency amplifier (LM371)—operates as a comparator and level shifter and drives a Schmitt trigger built with half a quad NOR gate (LU380A). The trigger switching threshold is centered at 2 volts above ground.

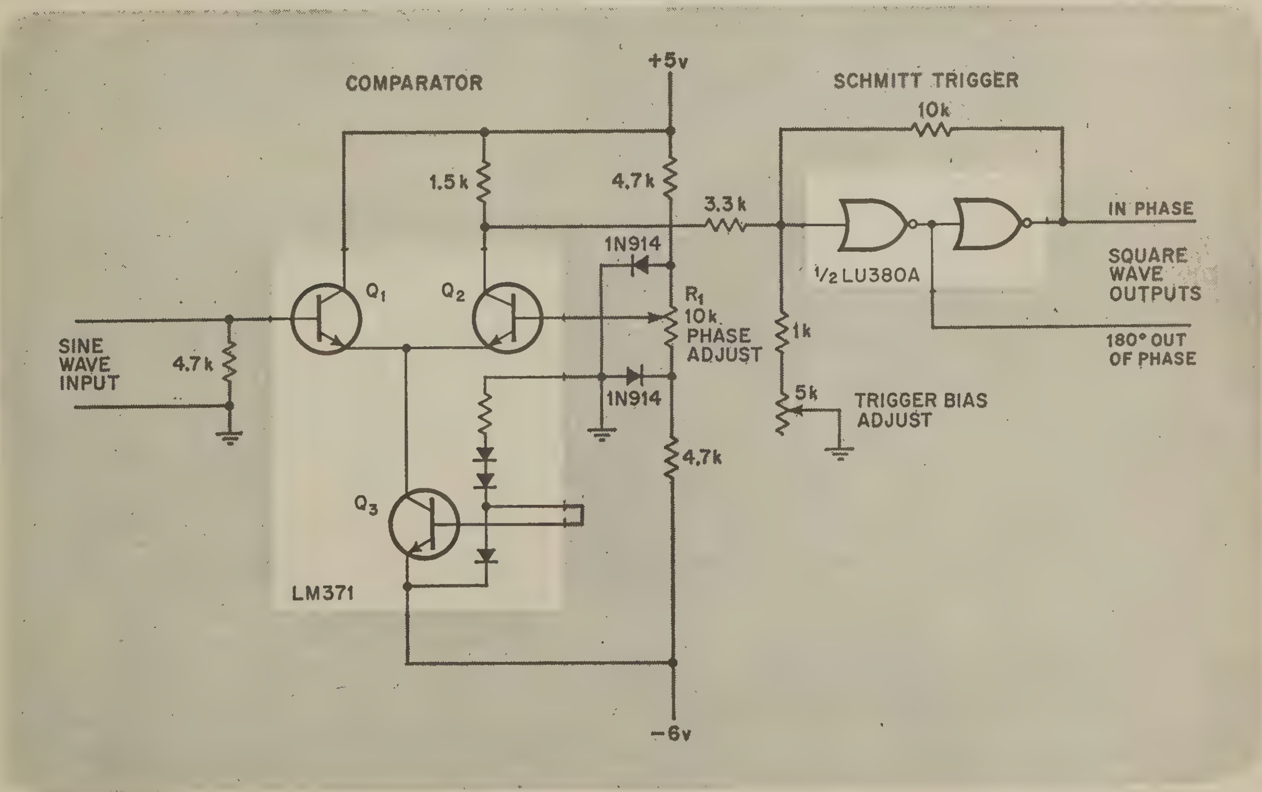
Differential transistor pair, Q_1 and Q_2, compare the analog signal with a d-c reference voltage. The amount of Q_2's collector voltage selected by the trigger bias potentiometer centers Q_2's output waveform in the trigger region. At small analog-signal amplitudes, the signal is amplified linearly and the Schmitt trigger shapes the sine wave into complementary square waves.

If the input-signal amplitudes become large, Q_1 and Q_2 go into current-mode limiting. This results in a square pulse of current which provides an ideal drive for the Schmitt trigger. Furthermore, the differential pair limits the Schmitt input thus minimizing phase variations in the trigger level.

However, the good common-mode rejection of the differential amplifier allows the d-c reference level to Q_2 to be varied. Potentiometer R_1 varies the level, effectively moving the comparison point up and down the slope of the sine wave. The levels of the square-wave output can be made to correspond to the axis crossings of the sine wave or any other discrete point with this adjustment.

As a result, inputs to the Schmitt trigger are shifted in phase by ±90° with respect to the sine-wave input. As the trigger's outputs are complementary, one or the other will provide any amount of phase shift desired from 0° to 360°.

Pulses with fast rise times can be generated even at low frequencies thanks to the direct coupling and snap action of the digital Schmitt trigger. Its operation was described in applications memos published by the Signetics Corp.



Shifty clipper. Besides limiting analog inputs to the trigger level, the comparator can be adjusted with R_1 to operate the trigger at any point on the sine-wave slope. Each complementary output can, in effect, be shifted ±90°, giving a total phase shift up to 360°. Output voltages are standard IC logic levels.

Diode-switched FET's rectify the full wave

By Leonard Accardi,

Kollsman Instrument Corp., Elmhurst, N.Y.

Unlike diodes, field effect transistors won't distort a signal sent through a full-wave rectifier bridge. Also, the FET bridge is controlled by an integrated circuit comparator, eliminating the usual transformer.

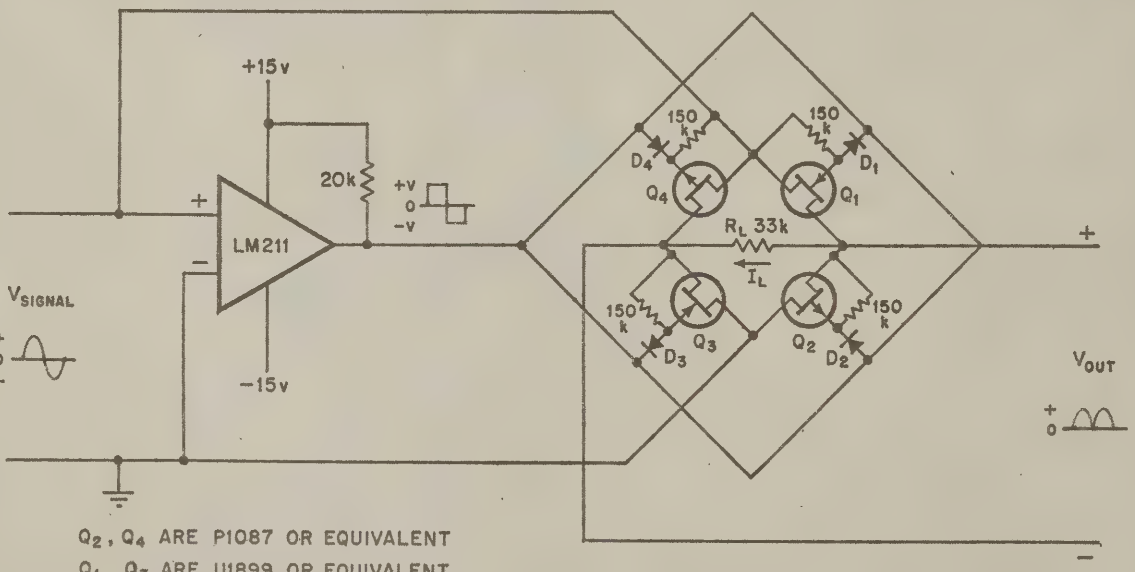
A conventional diode full-wave rectifier distorts output at low voltage due to the diodes' cut-in voltages. But with the FET's zero offset voltage, output closely follows or inverts each half of the sine-wave input signal.

The four diodes in the complete circuit do not rectify the signal. Instead, depending on whether the signal voltage is positive or negative, they switch the pairs of n-channel and p-channel FET's. The resistors connected across the gate and source of each FET insure that the gate-to-source capacitance discharges when the comparator voltage switches. Comparator A_1 is referenced to ground and biased such that the positive and negative switching voltages are always greater than the maximum signal voltage and the pinch-off voltage of the field effect transistors.

When a positive signal is applied, the comparator's +15 volts output reverse-biases diodes D_1 and D_3. This allows the n-channel FET's, Q_1 and Q_3, to turn on because their gates now float. However, the p-channel FET's Q_2 and Q_4, are held off because the forward-biased diodes D_2 and D_4 allow their gate voltage to go positive with respect to their sources. The positive portion of the input signal is conducted through Q_1, the load R_L, and Q_3 to ground.

The process is simply reversed for a negative input signal. The n-channel FET's, Q_1 and Q_3, are turned off and the current through the load R_L flows through Q_2 and Q_4.

Since the load current, I_L, always flows in the same direction, full-wave rectification is provided. The input signal voltage is impressed across the load resistor and whichever pair of FET's are conducting. How much of the input signal appears across the load resistor depends on the ratio of R_L and the ON resistances of the FET's. Since the FET's are switched directly by a square wave at some large input voltage, spikes resulting from capacitance feedthrough in the FET's parasitic capacitance would be seen in the output, if the circuit weren't driven from a low-impedance source—less than several hundred ohms. Also, using FET's with very low input capacitance would reduce the amount of switching voltage coupled into the load.



Q_2, Q_4 ARE P1087 OR EQUIVALENT

Q_1, Q_3 ARE U1899 OR EQUIVALENT

D_1 THRU D_4 ARE 1N3064 OR EQUIVALENT

No distortion. Full-wave rectifier design demotes bridge diodes to secondary role of switching the field effect transistor. FET's Q_1 and Q_3 conduct the positive half of the input signal, and Q_2 and Q_4 conduct the negative half. Since the FET's have no offset voltage, they do not distort the output.

Preset pulse train checks sequential logic

By Bruce M. Smith

University of Virginia
Biomedical Engineering division, Charlottesville

Testing clocked sequential logic circuits is easier with a pulse generator that can be set to produce a train of any number of pulses. The states of the logic circuits then can be checked after the preset number of input pulses are applied. With six integrated circuit packages and two 10-position, 4-pole rotary switches, the number of pulses can be set to any number between 1 and 99.

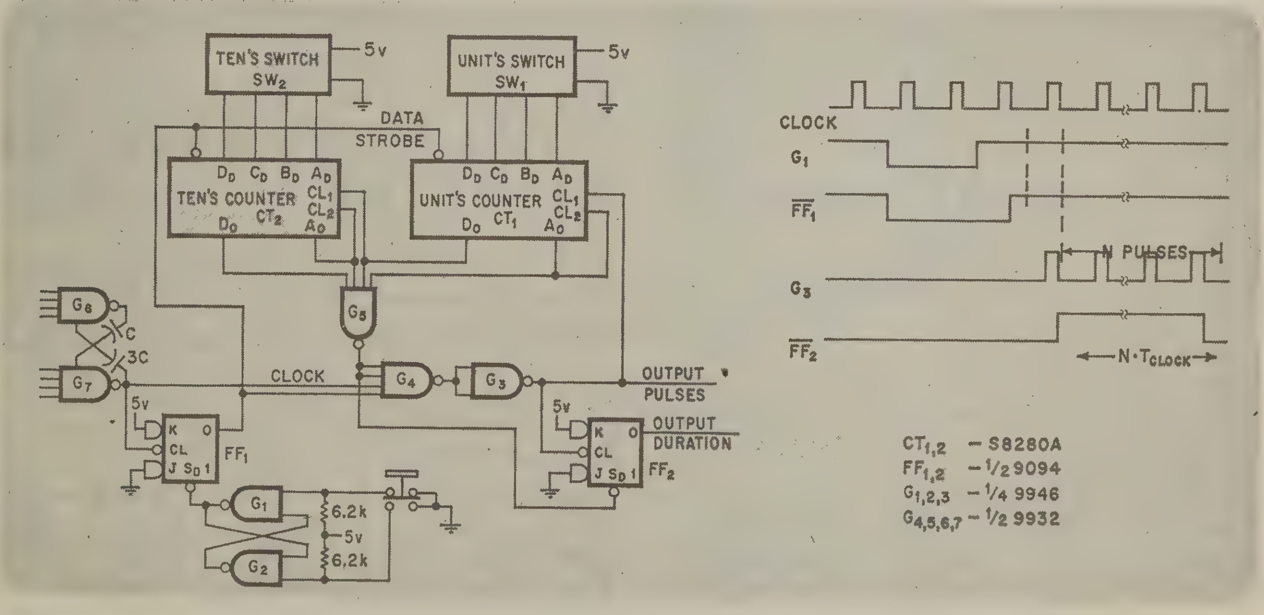
The rotary switches are wired to give the nine's complement, in binary-coded decimal format, of the selected number of output pulses. The clock can be obtained from gates wired as an astable multivibrator, as shown, or from an external source.

After the rotary switches are set, the pushbutton is depressed; the circuit generates pulses when it's released. Upon depression, the G_1-G_2 latch, used to prevent effects of contact bounce, sets FF_1. This causes FF_1's 0 output to go low, removing enabling input from G_4. The FF_1 0 output also acts as data strobe input to the counters and enters the switch information into the counters—the nine's complement of the desired number of pulses (the counter will actually count from this number to 99, thus producing the number of pulses as set on the switches).

The first clock pulse following the release of the pushbutton resets FF_1, which enables G_4 and the decade counters. Beginning with the next clock pulse, output pulses appear and are counted by the counters. The use of a clocked flip flop FF_1 guarantees that all output pulses will have the same width regardless of the timing of the asynchronous release of the pushbutton.

Output pulses continue until the counters reach 99. At this time, both D_0 and A_0 of each counter are 1's. This causes the output of G_5 to go low so that G_4 turns off and blocks the flow of clock pulses to the output. The circuit then stays in that state until the pushbutton is depressed again, either with or without changing the settings on the two rotary switches.

The extra flip-flop FF_2 yields an output pulse whose width equals the time taken by the preset number of clock pulses.



Pulse train. The number of pulses in the pulse train is set with the two rotary switches, which fix the starting point for the two counters. When the pushbutton is released, the clock pulses flow to the output through G_4 and G_3 and also are counted. When the counters reach 99, G_5 turns off, blocking the pulses.

Feedback triggers one-shot from both polarity edges

By P.B. Weil

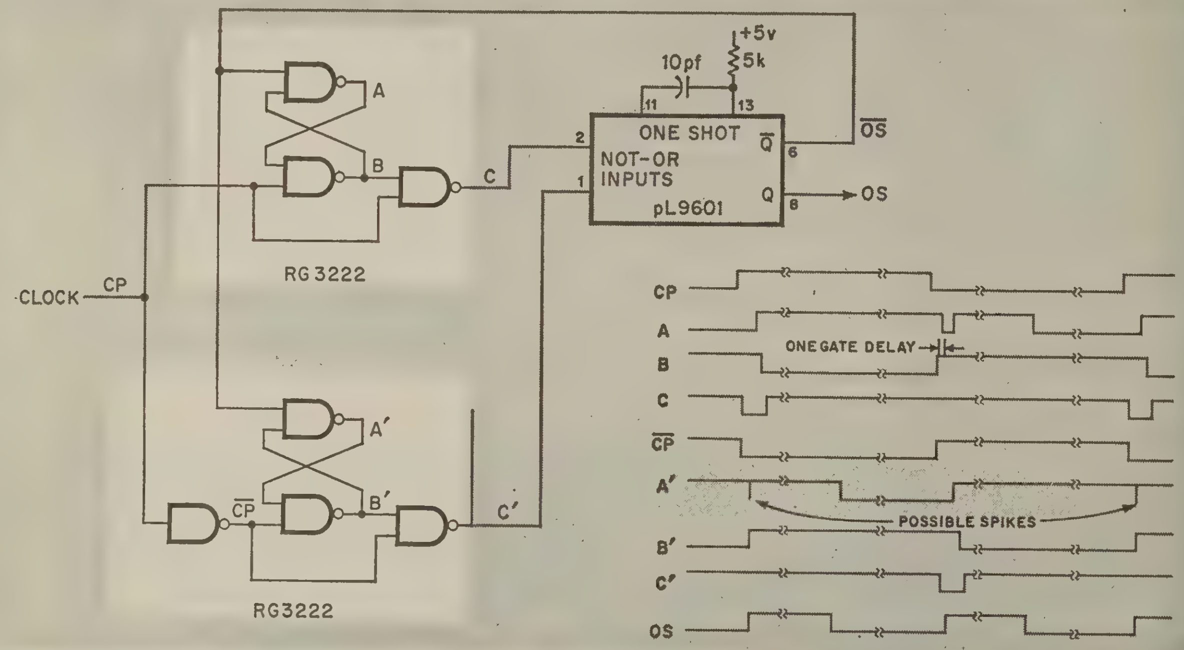
Hughes Aircraft Co., Culver City, Calif.

When it's necessary to trigger a one-shot on both edges of a clock signal, the schemes that come to mind first likely are simple differentiator circuits or two additional one-shots. But such devices use large components that may be incompatible with integrated circuit packaging methods and may introduce their own timing problems. And the differentiator may be susceptible to noise. A better method is to use a set of integrated gates connected as flip-flops and to take feedback from the one-shot back into the triggering circuit.

The circuit produces a trigger whenever the clock changes state. When the feedback shows that the trigger has done its job, the trigger pulse is turned off. The one-shot's pulse length is set at a quarter of the clock period. Thus, when triggered on both clock edges, it produces a signal at twice the clock frequency.

As the waveforms show, when the clock pulse is about to go high, flip-flop A-B has been set with B high. When CP does go high, output C goes low, firing the one-shot, within only two gate delays. When the one-shot output $\overline{\text{OS}}$ goes low, the flip-flop A-B is reset, putting B in the low state, and forcing trigger pulse C to return to the high state within three gate delays after firing.

When the clock goes from high to low, a similar action takes place in the A′-B′ flip-flop. Here, C′ acts as the trigger pulse.



On edge. The one-shot is triggered on each edge of the clock signal—when the clock goes from low to high, the one-shot switches and one of its outputs is fed back to A-B to turn off the trigger pulse. When the opposite clock transition occurs, the lower flip-flop produces the trigger pulse.

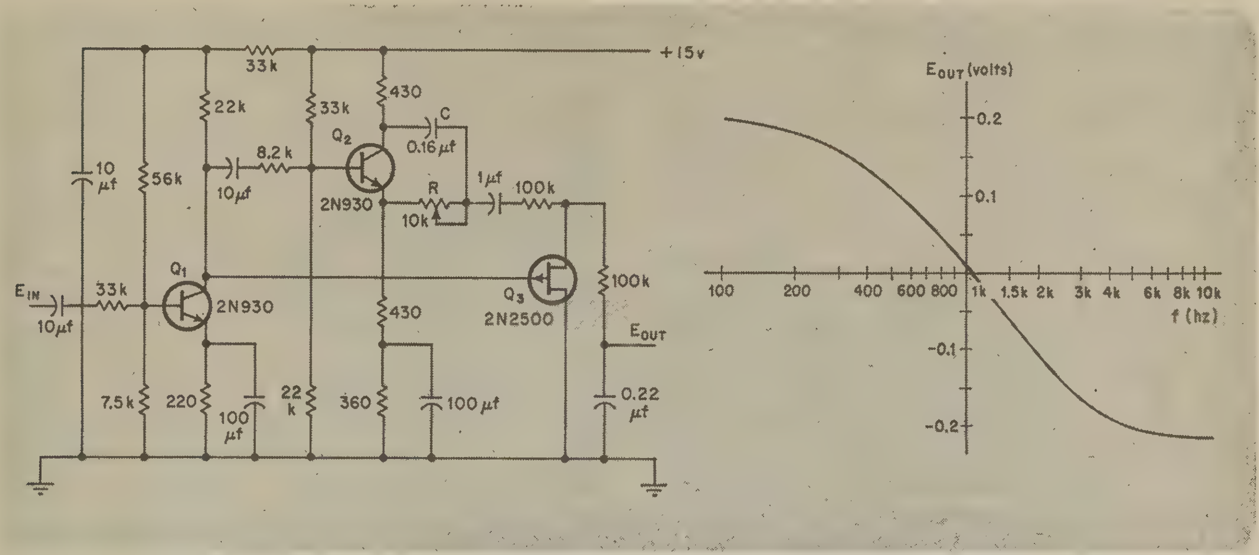
FET phase detector can be frequency-voltage converter

By Jerzy Kalinski

Unipan Scientific Instruments, Warsaw, Poland

A field-effect transistor with phase-shifted inputs to its gate and source, when used as a phase-sensitive detector, can deliver an output voltage proportional to the input frequency. As a frequency-to-voltage converter, it is useful in frequency meters and in measuring carrier frequency drift of higher r-f signals after demodulation. The FET circuit is particularly valuable in the audio-frequency range, where other methods using simple capacitor-charge measurements may be inaccurate.

The amount of phase shift depends on frequency; for one particular frequency, adjustable with potentiometer R, phase shift will be 90°. At this frequency, the d-c output voltage of the phase sensitive detector is zero. Frequencies that are lower than this center value voltage produce a positive voltage, while higher frequencies produce a negative voltage at the output.



FET detector. The field-effect transistor produces maximum voltage when its gate and source voltages are in phase or 180° out of phase; 90° phase shift gives zero voltage. Phase shift through the RC network depends on frequency and can be zeroed with the variable resistance.

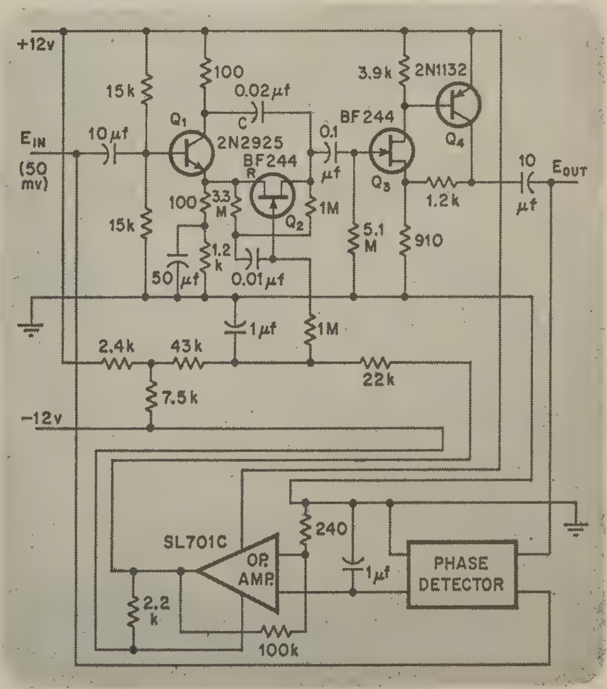
Variable FET resistance gives 90° phase shifts

By Jerzy Kalinski

Unipan Scientific Instruments, Warsaw, Poland

Frequency-independent phase shifters that produce 90° shifts in the audio-frequency range are useful for producing circular sweeps on a cathode-ray tube. They also can be employed in phase-measuring methods where a calibrated 0-to-90° phase shifter is formed by adding a signal to the quadrature component. A field-effect transistor can be used as the variable resistance in the RC phase shifter; FET resistance is controlled by feedback from a phase detector and operational amplifier.

In the circuit, the phase shift will be 90° when the reactance of capacitor C is equal to resistance R, the FET's source-drain resistance. When the phase shift tends to move off the 90° point due to a frequency shift, the phase detector produces an output of the proper polarity to bring the phase shift back to 90°.



FET setter. Field-effect transistor resistance sets the RC phase shift to 90°. FET resistance is controlled by the phase detector-amplifier combination.

IC oscillation sets up a mini-sized bias supply

By James Kotas

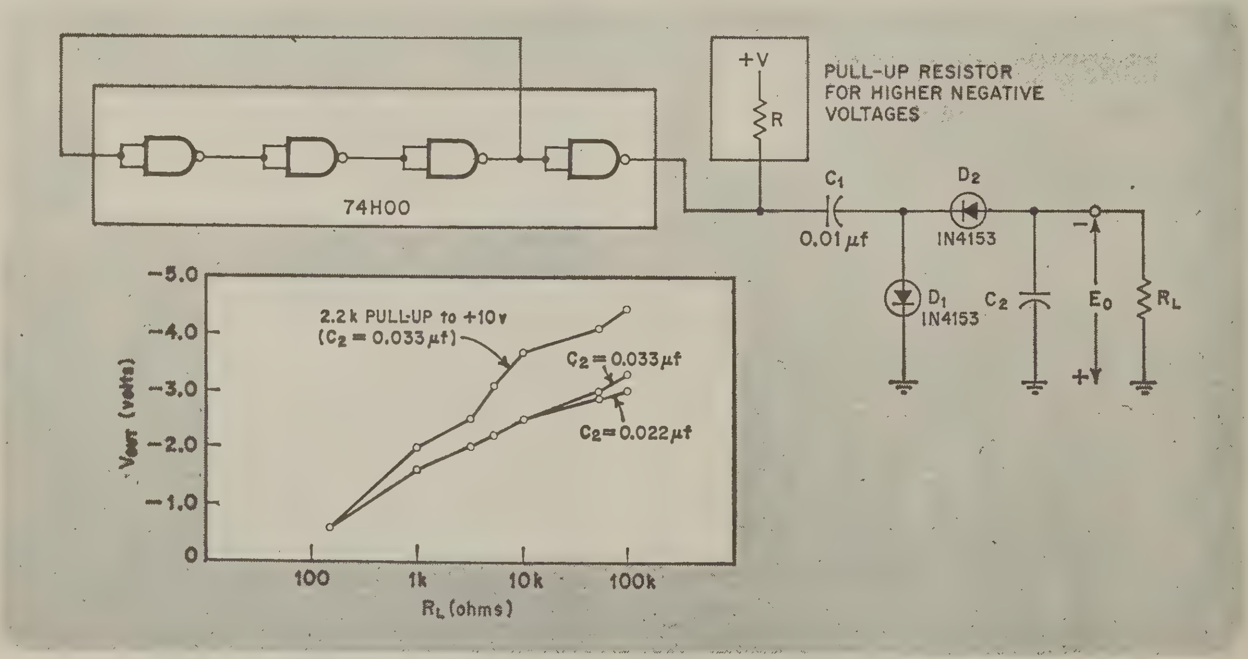
General Electric Co., Daytona, Fla.

Many circuits require a negative bias supply to give higher speeds in the cutoff of a transistor stage. But in small systems, it's often not economical to provide the necessary extra transformer winding and circuitry in the power supply. In a small test unit for checking memory operation, for example, a negative voltage was needed to speed up the clock circuit. With only a single integrated circuit package—a quad NAND gate—and two diodes, and two capacitors, the negative voltage was obtained.

Three of the NAND gates are connected in a loop to form an astable multivibrator, which, with transistor-transistor logic circuits, will oscillate at about 33 megahertz. The output of the fourth gate applies the square wave, running from about 0.2 volt up to about 4 volts, to the capacitor-diode circuits.

When the output of the gate is high, C_1 charges through D_1 to 4 volts, minus the diode voltage drop, or about 3.3 volts. When the gate output drops, capacitor C_1 is effectively placed across D_1, cutting it off. In addition C_2 charges through D_2 to the voltage on C_1, minus the D_2 voltage drop and the 0.2 volt, for the low level. The C_2 voltage, however, is negative with respect to ground, and its net value is about —2.4 volts. A higher negative voltage can be obtained by connecting a pull-up resistor to a higher positive voltage at the output of the fourth gate.

The test units uses TTL circuitry because of the lower delays. If diode-transistor logic had been used, the oscillator frequency would have been in the 10-Mhz range, introducing more ripple in the d-c output. The value of C_2 is not critical and could be eliminated with high impedance loads.



Mini bias. Three NAND gates form an astable multivibrator oscillating at about 33 Mhz, while the fourth gate drives the capacitor-diode network. Capacitor C_1 charges when the gate output is high and transfers its charge to C_2 when the gate output goes low. The output voltage is negative with respect to ground.

Switching regulator drives IC's and Nixies off battery

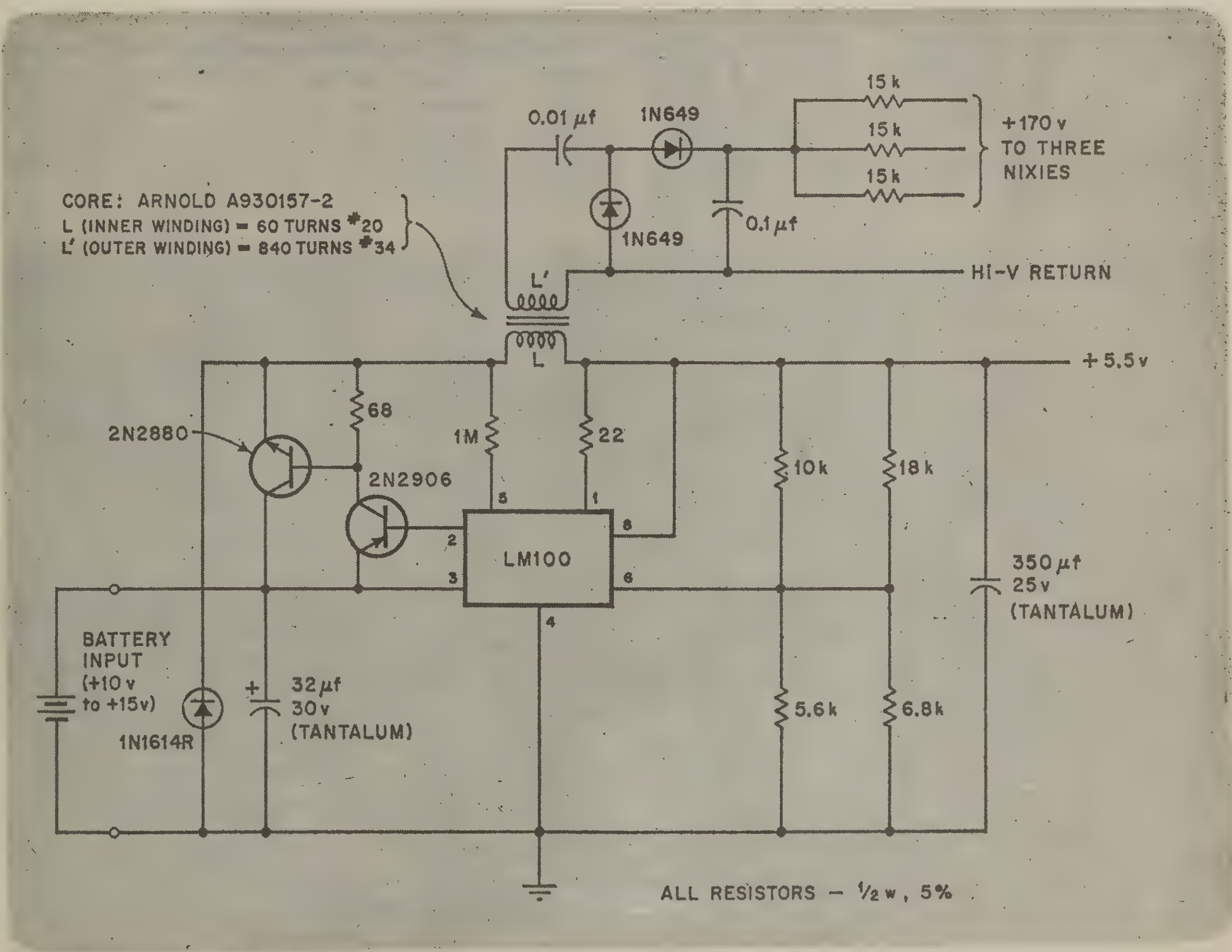
By David B. Newton

U.S. Army Electronics Command, Fort Monmouth, N.J.

The combination of integrated circuits and Nixie tubes is one that's widely found in digital instruments. Yet the large difference in supply voltages needed for the two can pose a problem when designing a power supply for equipment that must be battery operated for portability. With a battery-operated supply, any voltage converter that's used should have a high efficiency to conserve battery energy. This can be accomplished with a switching regulator built around an integrated regulator circuit, the LM100, and both an extra winding on the smoothing inductor and a voltage doubler to obtain the high voltage for the Nixie tubes.

The basic regulator circuit bears some similarity to one described by the manufacturer in an application note, but in this case, the input and output capacitances have been increased. This increase was found to be necessary to improve the efficiency when the extra winding was added to the smoothing inductor. Without the change in capacitor values, the switching frequency was higher and the extra winding caused the regulator to lose its sharpness in turnon and turnoff. With the 22 microfarads and 100 μf recommended, the switching frequency would be between 30 and 75 kilohertz. With the values shown—32 μf and 350 μf—the frequency drops to about 9.8 khz, and efficiency is in the 78% to 85% range, depending on the low-voltage load.

The circuit produces two separate output voltages for an input voltage of from 10 to 15 volts. The TTL logic circuits are supplied 5.5 volts, regulated to within ±1%, for load currents from 0.1 to 2 amperes. Maximum noise voltage is 0.5 volt peak-to-peak. Driving the three Nixie tubes takes from 150 to 210 volts at about 6 millions.



Nixie power. The extra winding on the switching regulator's smoothing inductor drives a voltage doubler to provide the 150 to 210 volts needed for Nixie display tubes. The circuit also produces a low voltage for powering transistor-transistor logic circuits. Overall efficiency is between 78% and 85%.

Switched oscillator controls four-wire resistance checks

By C.H. Ristad

International Business Machines Corp., Endicott, N.Y. . .

Computer-controlled component testing requires an array of switches that apply a voltage or current drive to the component and also connect an appropriate meter into the circuit. In four-wire resistance measurements, for example, a current source is applied and the voltage is monitored across the component terminals. However, accuracy requires separate grounds for the switching and component measurement circuits. And for high testing rates, the switch should operate at high switching speeds.

This circuit gets the needed isolation from a shielded transformer, which is driven by an oscillator that's switched on by the gate circuit. The current and voltage switches are then turned on by the rectified oscillator signal from the transformer's secondary winding.

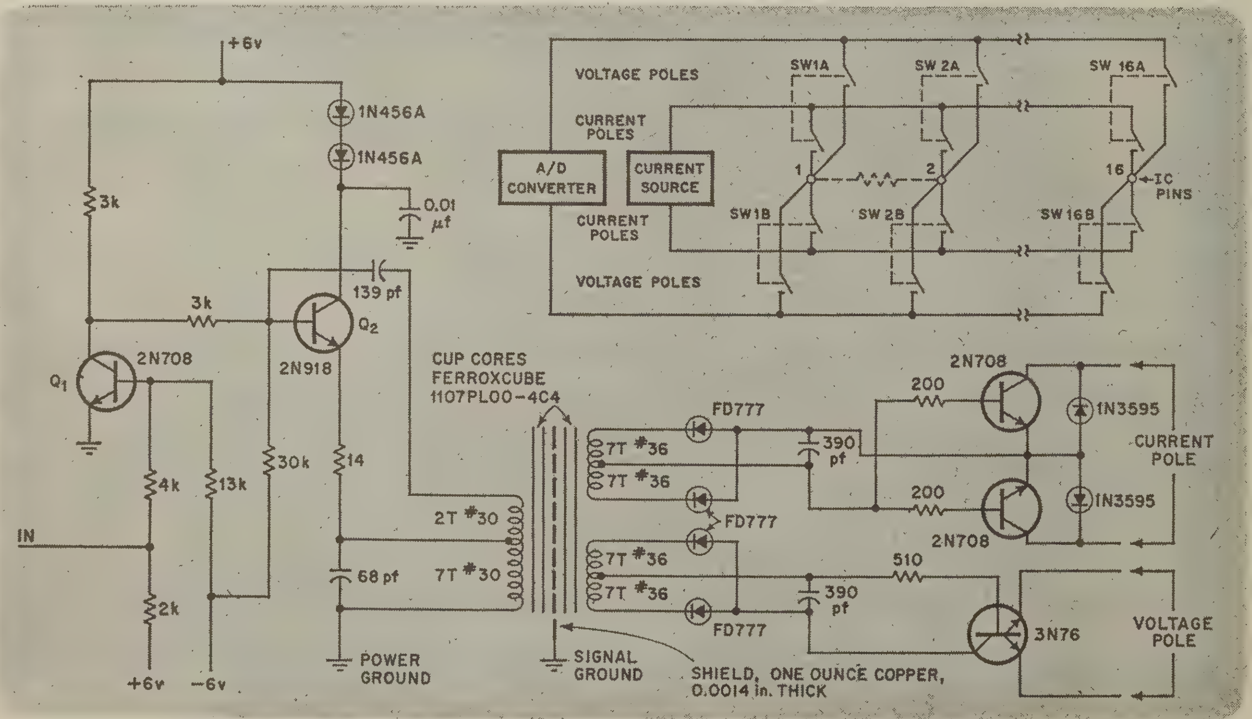
To measure the resistor between pins 1 and 2 of the integrated circuit; switches 1A and 2B are turned on. This allows current flow and connects the terminals to the analog-to-digital converter for voltage measurement. To reverse the current—as in measuring the reverse resistance of a diode—switches 1B and 2A are turned on.

An input signal of zero volt grounds the 2-kilohm resistor in the base circuit of Q_1, and Q_1 turns off. Transistor Q_2 then turns on, oscillating in the 14-megahertz Hartley circuit. The current and voltage switches then turn on. Turn-on time is about 2 microseconds. A 6-volt input allows base current to flow in Q_1, Q_2 turns off, and the oscillation ceases, opening the current and voltage switches.

The transformer's primary and secondary windings are on separate bobbins and are physically separated in the cup cores. A thin sheet of copper, sandwiched between the cup cores, acts as an electrostatic shield.

Currents up to 100 milliamperes can flow in the current circuit because the two shunt diodes act to eliminate the need to operate each transistor in the inverse mode, where current-carrying ability is lower than in the normal mode. The 3N76 dual emitter, integrated chopper transistor in the voltage circuit provides lower offset voltage than two separate transistors.

Isolation is good for frequencies below 100 kilohertz, but at the 14-Mhz oscillator frequency, a nearly 1 volt peak-to-peak noise occurs in the output. However, this will be far above the passband of the a-d converter; but note that converters that rectify noise inputs would not be suitable in this case.



No common ground. The transformer provides isolation between switch control and measurement circuit grounds for four-wire resistance measurements. Transistor Q_2's circuit oscillates when turned on by Q_1's turnoff, and the transformer output is rectified to close the voltage and current poles of the switch.

Zeners cut corners in MOS gate driver

By Roland J. Turner

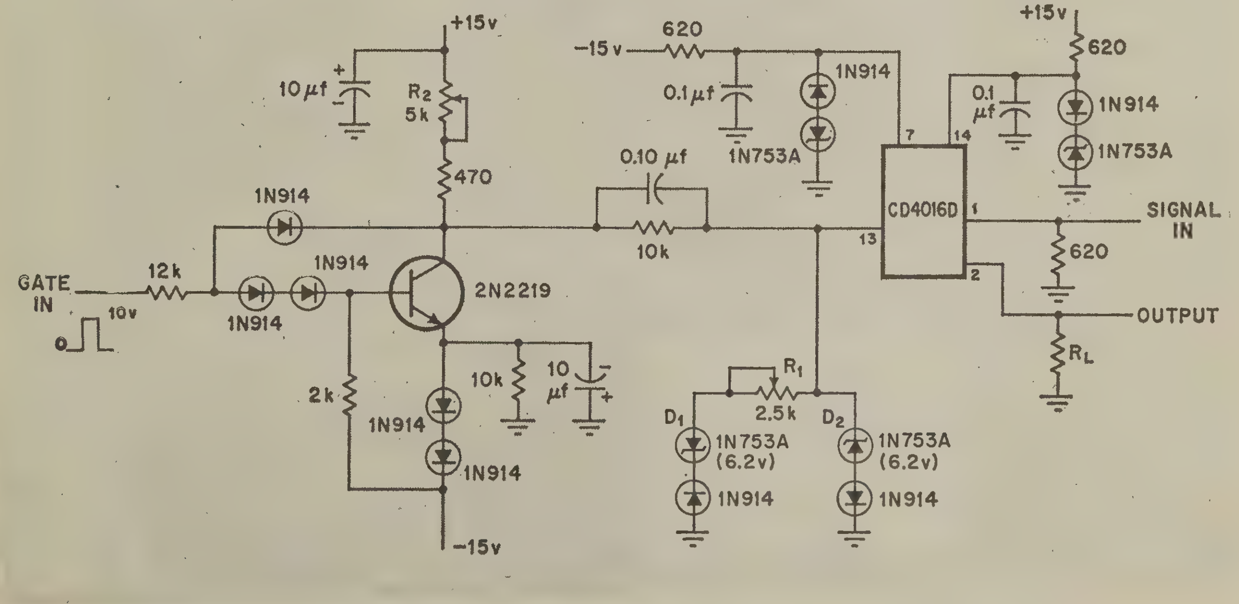
General Atronics, Philadelphia, Pa.

The availability of complementary-channel MOS sampling-gate circuits, such as RCA's CD4016D, earlier designated as the TA5460, provides the opportunity to increase the dynamic range of sample-and-hold circuits. But the drive circuits must be designed to take full advantage of C/MOS devices and achieve the reduced transients—the fundamental purpose of going complementary in this type circuit. A driver circuit was designed that achieves maximum transient peaks in the load that are 46 decibels down from the maximum gating amplitude, compared with transients as little as 20 db down without the circuit. Furthermore, the energy in such transients is very low—about 5 x 10^{-8} volts-second.

In an exponential drive waveform, the sudden changes of slope at the beginning of the rise and at the top of the pulse are the major sources of transients that could be coupled to the load through the gate-to-load capacitance. The drive waveform would be better if it had no slope discontinuities and if it had as low a turn-on and turn-off slope as possible, while still gating within the desired time interval.

Zener diodes with series resistance round off the corners of the drive waveform. In addition, a nonsaturating drive switch prevents direct feedthrough of the input waveform—a condition that would exist in a saturating switch driver due to the coupling from input to output.

The waveform at the collector of the nonsaturating drive, the 2N2219, switches from +15 volts to −14 volts and drives the zener-diode shaping network to turn off the CD4016D gate. The collector waveform has sharp corners that are softened by D_1 and D_2 so that a smooth transition is presented to the gate input. The two diodes also limit the input swing applied to the CD4016D to about +7 volts and −7 volts (6.2-volt zener plus forward drop for the 1N914). R_1 is varied to adjust the off-going transient, and resistor R_2 takes care of the on-going transient.



Corner softener. The zener diodes, with their series resistances, will soften the sharp edges of the drive waveform applied to the complementary MOS switch. This softening reduces the transients that appear in the output waveform and thus increases the dynamic range of the switch.

Exclusive-OR IC's serve for phase-locking tasks

By George S. Oshiro

Teledyne Systems, Los Angeles, Calif.

An exclusive-OR circuit can serve as a simple phase detector in a phase-locked loop. The circuit is insensitive to noise because the control voltage is averaged and noise pulses have low d-c components. And it can be used from d-c to about 5 megahertz.

The inputs to the quad-gate exclusive-OR IC are the output signal, f_o, and the reference signal to which the output is locked. The exclusive-OR circuit's output is high (logic 1) when the reference and output signals are in the same states.

The resulting train of pulses is filtered to extract its d-c component. The d-c is amplified to set the frequency of the voltage-controlled oscillator.

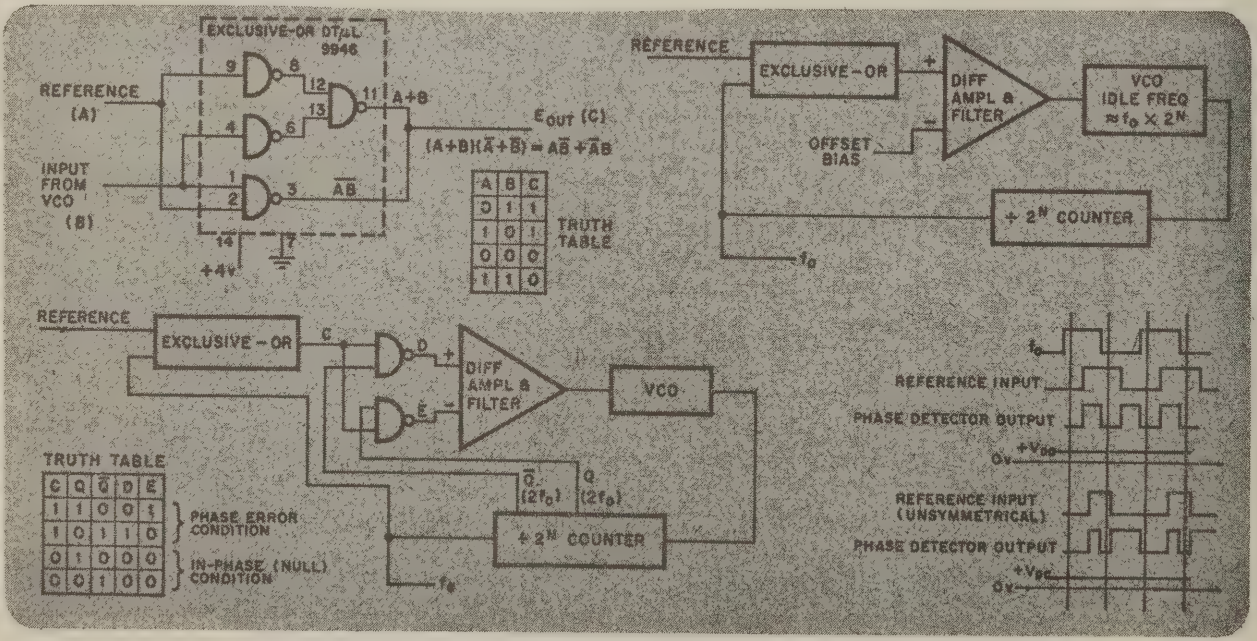
The d-c level corresponding to the desired frequency of the output is nulled out with an offset bias applied to the amplifier. Thus, when the output is at the desired frequency, the nominal, center-frequency voltage is applied to the voltage-controlled oscillator. If the output tends to increase in frequency, the exclusive-OR output increases its duty cycle; its d-c level increases, and this change in d-c voltage is transmitted to the VCO to decrease its frequency. Decreases in output frequencies are counteracted in a similar way.

In the circuit shown, the offset bias is set to make the reference and the output signals 90° out of phase—there will be 90° between the midpoints of the high part of the waveform. The VCO's frequency however, can be any factor 2^N times the reference frequency and must be divided down by the same factor to develop the output frequency. Thus the VCO's frequency can be higher than the reference, making design of the VCO easier.

With this scheme, the d-c component of the exclusive-OR output is independent of the reference's duty cycle, and thus small changes in the reference's symmetry are ignored if the reference signal frequency stays constant. Also, narrow noise pulses on the reference waveform are essentially ignored, since they will have only a small d-c component. However, because the offset bias is fixed, there can be a drift with temperature that would be interpreted as an error signal.

With two NAND gates added to the circuit, the drift problem can be eliminated because the outputs of the NAND gates will have similar temperature characteristics. In addition, this scheme provides an output that is in phase with the input.

With this setup, the truth table shows that when the exclusive-OR output is high—a logic 1—there is a phase-error condition. The exclusive-OR output will be high when the reference and the output signal are different, indicating that they are out of phase. When the exclusive-OR circuit output is low—logic 0—the reference and output are in phase and D and E are both low.



A	B	C
0	1	1
1	0	1
0	0	0
1	1	0

C	Q	$\bar{Q}$	D	E
1	1	0	0	1
1	0	1	1	0
0	1	0	0	0
0	0	1	0	0

Locking it in. The exclusive-OR circuit compares the signal output with the reference and delivers a train of pulses whose d-c value sets the frequency of the voltage-controlled oscillator. With two additional NAND gates, the circuit provides an output in phase with the input.

Dynamic braking emf signals motor to reverse

John E. Bjornholt

Motorola Government Electronics, Scottsdale, Ariz.

For years, d-c motors have been braked by placing a resistance across the motor after power is disconnected. But the voltage generated as the motor slows also can be used as a signal to set up the motor drive circuit for the next sequence of events. For example, in a motor-driven antenna, the generated voltage is used to provide the necessary switching to reverse the connections to the motor, thus switching its scan direction.

In the circuit, K_1 is a latching relay—it has two coils that need only be pulsed to move the contacts to the opposite position, where they remain until the next pulse to the opposite coil. Assume that coil L_1 had been pulsed last and the contacts are as shown. The motor is turning clockwise.

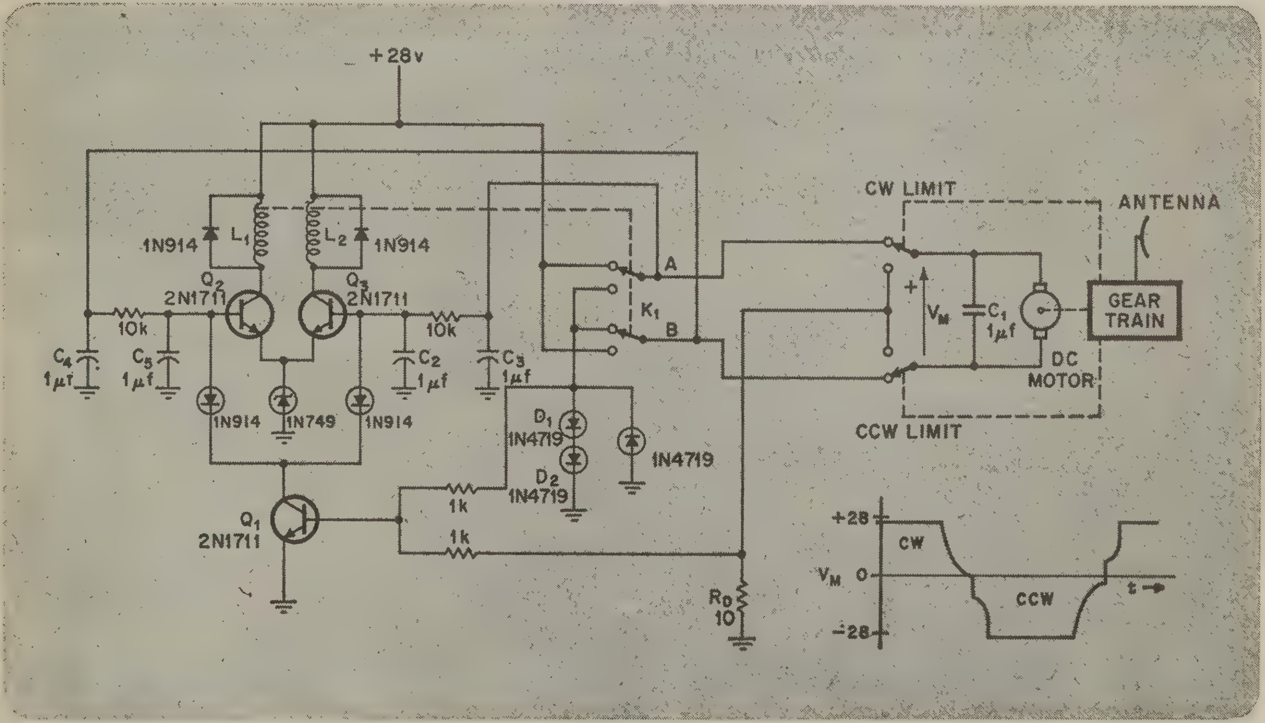
The motor is returned to ground through the diodes D_1 and D_2. The voltage across these diodes holds Q_1 on, which in turn holds both Q_2 and Q_3 off.

When the antenna reaches its limit, the cw limit switch is actuated, and the motor loses its 28-volt supply line. Inertia continues to turn the motor, but resistor R_D dissipates the inertial energy. The generated emf also is applied to the base of Q_1, holding it on. When the motor stops, Q_1 turns off and Q_3 turns on—the point A is still connected to the 28-volt supply through the switch.

This energizes L_2 and switches K_1, which reverses the voltage going to the motor, causing it to reverse. After K_1 switches, point A is connected to ground, Q_3 turns off, and Q_1 turns on again as current flows through the motor and through R_D (the cw limit switch hasn't switched yet). Thus, resistor R_D not only controls the damping of the motor, but it also limits the starting current to the motor. However, R_D does limit the motor's starting torque.

As the antenna backs off its full cw position, the cw limit switch goes back to its former position and current again flows through D_1 and D_2, keeping Q_1 on. A similar sequence of events occurs when the motor reaches its ccw limit.

Capacitors C_2 through C_5 keep the circuit from falsely actuating the relay during the time the limit switches and relay contacts are in the transitional state, while C_1 acts as a commutation noise filter on the motor. The damping resistor's size depends on the size of motor, but as a rule of thumb, it may be set at twice the armature resistance.



Hitting the brakes. The damping resistor, R_D, dissipates the inertial energy of the motor when power is disconnected and also develops the signal to turn on Q_1 as the motor is slowing down. When the motor stops, Q_3 turns on and pulses the latching relay to reverse the connections to the motor.

Build ring counters with standard MSI

By Wolfgang Nadler

University of Pennsylvania, Philadelphia

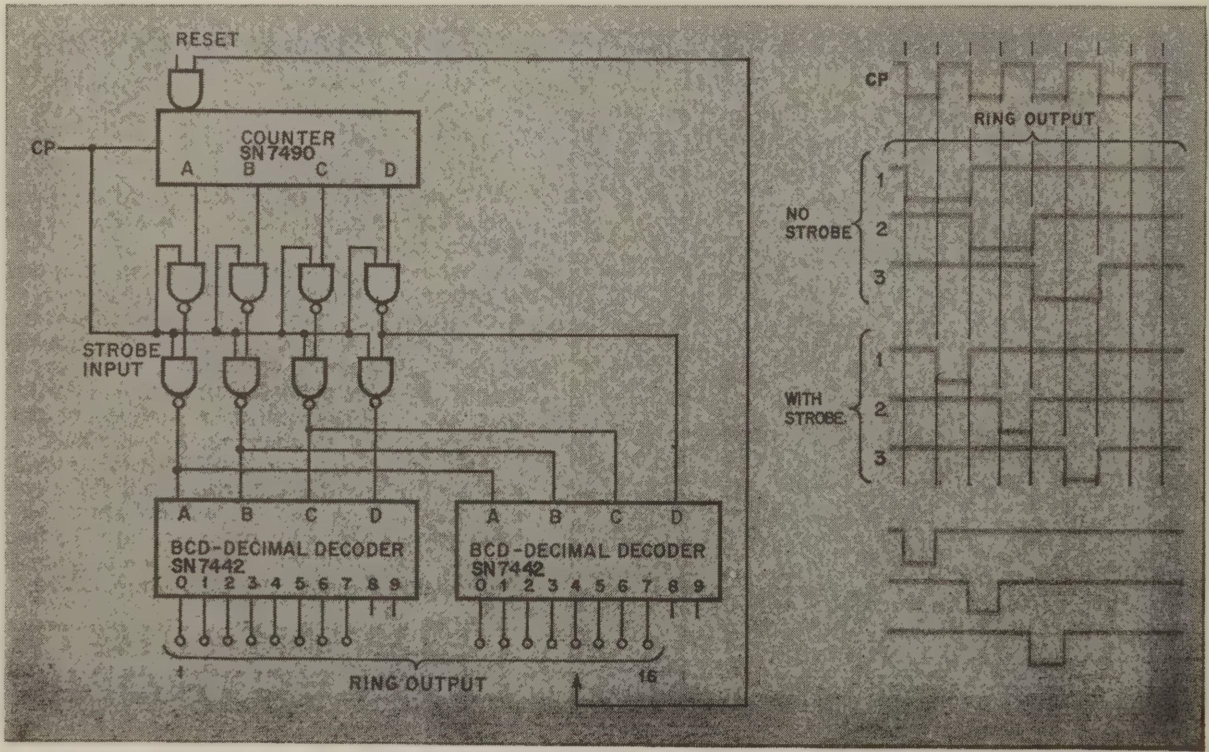
Only a few connections between standard medium-scale integrated circuits are needed to assemble a ring counter, based on a simple circuit that decodes the output of a binary counter. Since the decoding does not allow more than one output, only one pulse will go around in the ring, even if false triggering should occur.

The straight-binary, ripple-carry counter is driven by the clock pulses and in turn drives two decoding networks through appropriate gating circuits. One decoder generates outputs 0 to 7 while the other generates 8 to 15 by inverting the fourth-level binary output, input D. Reset can be taken from any output to determine the number of active stages in the ring.

A strobe input is required to prevent transient spikes which may be caused by the propagation delay between stages in the counter. The output pulses are 180° out of phase with the input train of pulses.

Only one decoder would be needed for a ring counter with 10 or less outputs, while a divide-by-12 counter would give a space of two clock pulses before the ring pulse repeats. The direct feedback for reset can be used with any configuration and will always take up one ring output interval of time.

In the circuit shown, outputs 8 and 9 of the decoders are not used because they are the same as the 0 and 1 outputs of the other counter and thus would be redundant.



Around the ring. The ring counter uses a basic straight-binary counter to drive two decoders, which provide a pulse that steps in sequence through each of the output lines. The number of stages in the ring is variable and can be set by taking the reset off any of the output lines.

Telemetry signal conditioner centers its slicing level

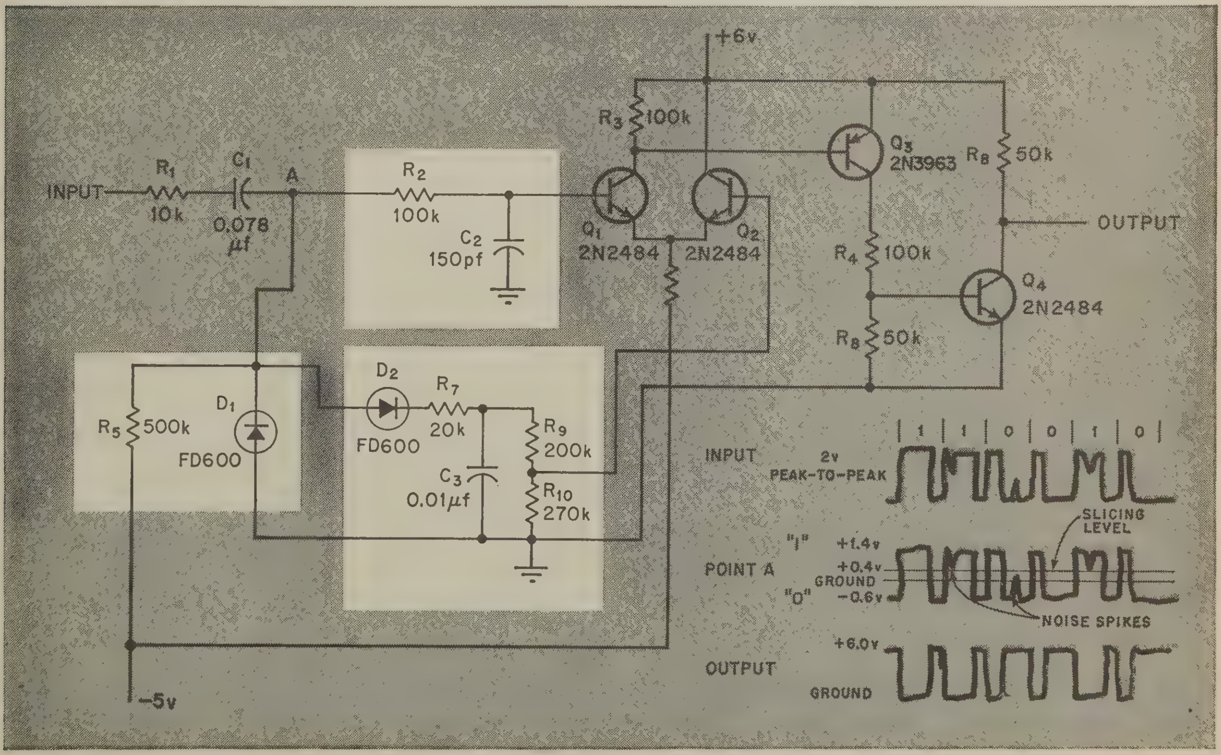
By Jeff Schlageter

Fairchild Semiconductor, Mountain View, Calif.

A noisy telemetry signal can be conditioned for optimum signal-to-noise performance by slicing away the noise. This technique can result in an 8-decibel signal-to-noise ratio, a 10-db improvement over circuits previously used. In telemetry a common method of coherent bit detection is to filter the incoming signal before sampling. However, filtering is not very effective in cases where the signal frequency falls within the noise bandwidth. In that case, the signal conditioner described here may be preferred over the filter. The circuit features a slicing level that automatically adjusts itself to the center of the input signal amplitude, is minisized, has a 200 microwatt standby power, and can handle signals from 2 to 5 volts peak-to-peak.

The signal is fed through an impedance matching resistor, R_1, to one input of a differential amplifier Q_1—Q_2. The other differential amplifier input is biased at a potential that is exactly one half the peak-to-peak input signal amplitude by the network consisting of D_1, R_5, D_2, R_7, C_3, R_9, R_{10}. Diode D_1 is biased by resistor R_5 to provide a negative reference for point A, thus, effectively clamping the input to that level. Diode D_2 rectifies the input signal and charges up C_3 to almost the peak signal voltage level. Then, when properly chosen, R_9 and R_{10} divide this level to one half the input peak-to-peak signal amplitude with respect to point A and apply it to the base of Q_2. Consequently, an input signal variation a few millivolts above or below this level at the base of Q_1 will drive Q_4 to full output swing and appear at the output as an inverted but noise-free replica of the input. The circuit exhibits good stability with temperature variation.

The choice of circuit element values depends on the frequency of the input signal. This circuit was designed for an input signal of 4 kilohertz, and although it will work over a wide range of input frequencies, certain precautions should be observed when deviating from the design. For example, the charging time of capacitor C_3 through D_2 and R_7 must be much shorter than the discharge time through R_9 and R_{10}. Also, the discharge time of C_3 should be long compared to the period of the input signal. To avoid excessive droop at point A, the discharge time of C_1 through R_5 must be long compared to the positive input pulse width.



Sliced thin. The noise in a telemetry signal is sliced away by driving the output to its full value when the input varies from its nominal level by only a few millivolts. Transistors Q_1 and Q_2 form a differential amplifier with inputs of the signal itself and one half the peak-to-peak value of the input.

Comparator and a-c coupling provide d-c transformer action

By Thomas J. Carmody

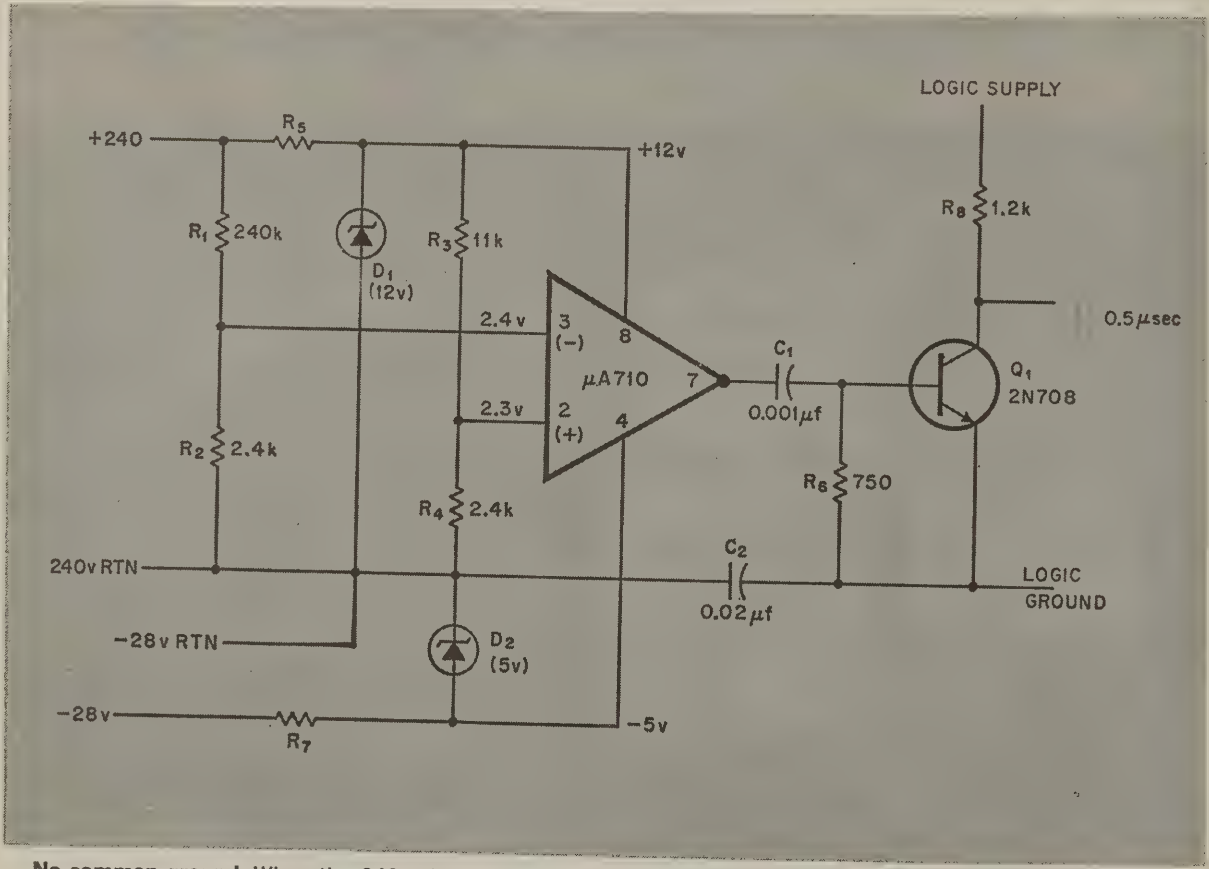
PRD Electronics Inc., Westbury, N.Y.

One way to avoid problems arising because of different grounds in a-c systems is to use a transformer for isolation. For d-c circuits, however, it's not so easy to go to the shelf and take down a d-c transformer. Consider the case where a control signal is to energize logic circuits when a power supply's voltage drops below a certain value. The power supply is operating at 120 volts above ground, and the control logic is referenced to ground. To transform the high voltages to the 5-volt d-c logic level and to provide isolation, a comparator circuit with a-c coupling to the logic circuit is used as the d-c transformer.

The 240-volt supply output is divided down by R_1 and R_2 so that 2.4 volts is applied to the inverting terminal of the integrated comparator. The comparator gets its reference and supply voltages by tapping off the supply with a zener diode and current-limiting resistor. The 12-volt comparator reference is set by the zener, and stepped down by R_3 and R_4 to a constant 2.3 volts, which is applied to the positive input of the comparator. When the high-voltage drops below 230 volts, the inverting input drops below 2.3 volts and the comparator output rises since the comparator's non-inverting input—2.3 volts—is now higher than the voltage applied to the inverting input.

This rapidly changing leading edge is a-c coupled through C_1, which also provides d-c isolation, and differentiated to produce a positive pulse to turn on Q_1. The output of Q_1 drives the compatible logic, which, in turn, provides the required control action. C_2 isolates the d-c grounding systems and is also made large compared with C_1 to provide a low-impedance return for differentiated signals.

The current limiting resistor, R_5, supplies a current of 12 milliamperes to the comparator. The —5-volt supply for the comparator is, in this case, tapped off a negative supply that shares a common return with the 240-volt supply.



No common ground. When the 240-volt supply voltage drops below 230 volts, less than 2.3 volts is applied to the inverting input of the comparator. The comparator then switches because its reference level is set at 2.3 volts. The a-c coupling isolates the high-voltage from the low-voltage output logic.

Matched FET's stabilize amplifier's bandwidth

By G. Fontaine and G. Reboul

College de France, Paris

Matched field effect transistors allow the designer to build variable gain amplifiers while maintaining a constant bandwidth throughout the range of gains for the amplifier.

The gain of the amplifier, K, is defined as the ratio, R_2/R_1, where R_1 is the FET's variable resistance defined by the voltage on the FET Q_1's gate. Thus, the input-gate voltage to the FET controls the gain of the amplifier.

However, it is the phase-lag compensation rather than the gain that causes the problem. The open-loop gain of the amplifier is a function of frequency and decreases proportionately to 1/f when using a lag compensation. As such, the amplifier's bandwidth varies as $1/(1+K)$. Thus for a value of $K=1$, the bandwidth is 5 megahertz, while for $K=100$ the bandwidth is 100 kilohertz.

One good approach to stabilizing the bandwidth is to design an input lag-compensation network. Assuming $R_i < R_1$, the solution to the bandwidth can be obtained from the equation

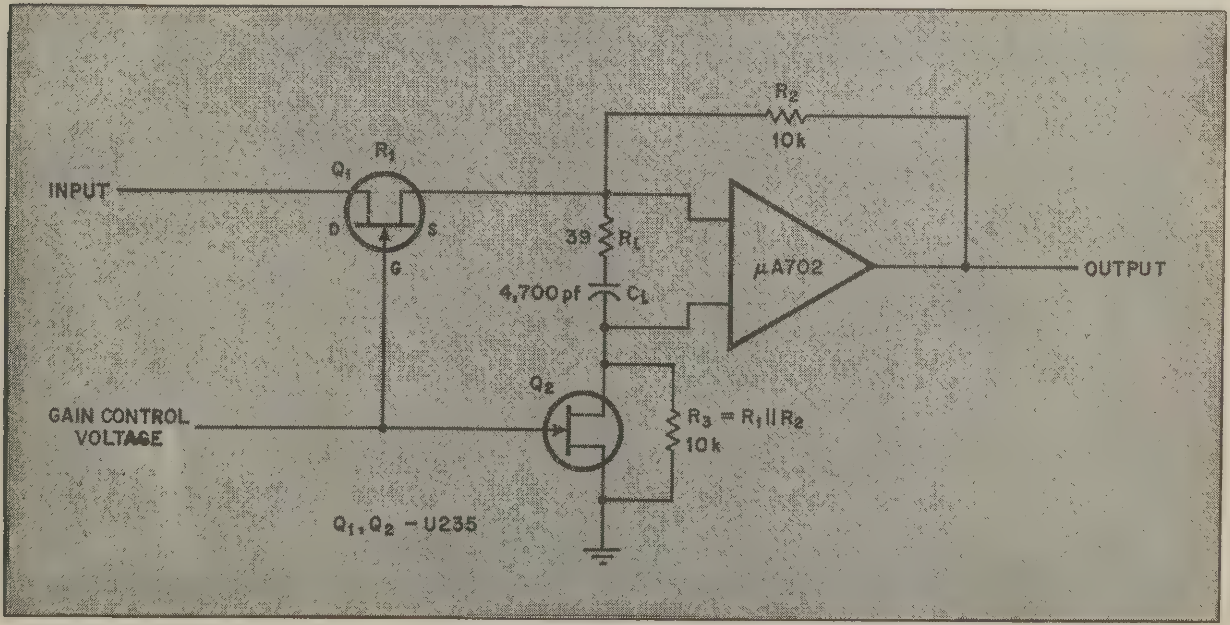
$$|A(f)| = \frac{R_2 + R_3(1+K)}{R_i}$$

To prevent the bandwidth from varying with the gain, K, the term, $R_3\,(1+K)$, must either be canceled or made constant.

If R_3 is made equal to 0, bias and offset effects are left uncorrected. However, a solution can be arrived at by making the term a constant. If R_3 is set proportional to $1/(1+K)$, the gain becomes independent of frequency.

Since $1/(1+K)$ is equivalent to $R_1/(R_1+R_2)$, R_3 can be chosen to have a value $R_1R_2/(R_1+R_2)$, where R_2 is a fixed value. This can be readily implemented using for R_3 a resistance equal to R_2 in parallel with a FET matched to R_1.

Since the same gate voltage controls both FET's, the R_3 term in the equation for the bandwidth remains almost constant, allowing a wide selection of gains without severely affecting the bandwidth.



Input compensation. Making the resistance, R_3, equal to the parallel combination of R_1 and R_2 compensates for the phase lag of the amplifier over various values of gain. Bandwidth remains unaffected since the same gate voltage controls channel resistances of both field-effect transistors.

Q-multiplier analyzes audio-frequency tones

By Roland J. Turner

Magnavox Co., Philadelphia

One effective way to analyze phase-modulated frequency tones is to use a gated Q-multiplier as an active bandpass filter. The Q-multiplier integrates, stores, and analyzes audio tones, which can be separated by as little as 80 hertz with a crosstalk level below 46 decibels. This approach allows many information channels to be densely packed leading to more efficient use of the frequency spectrum.

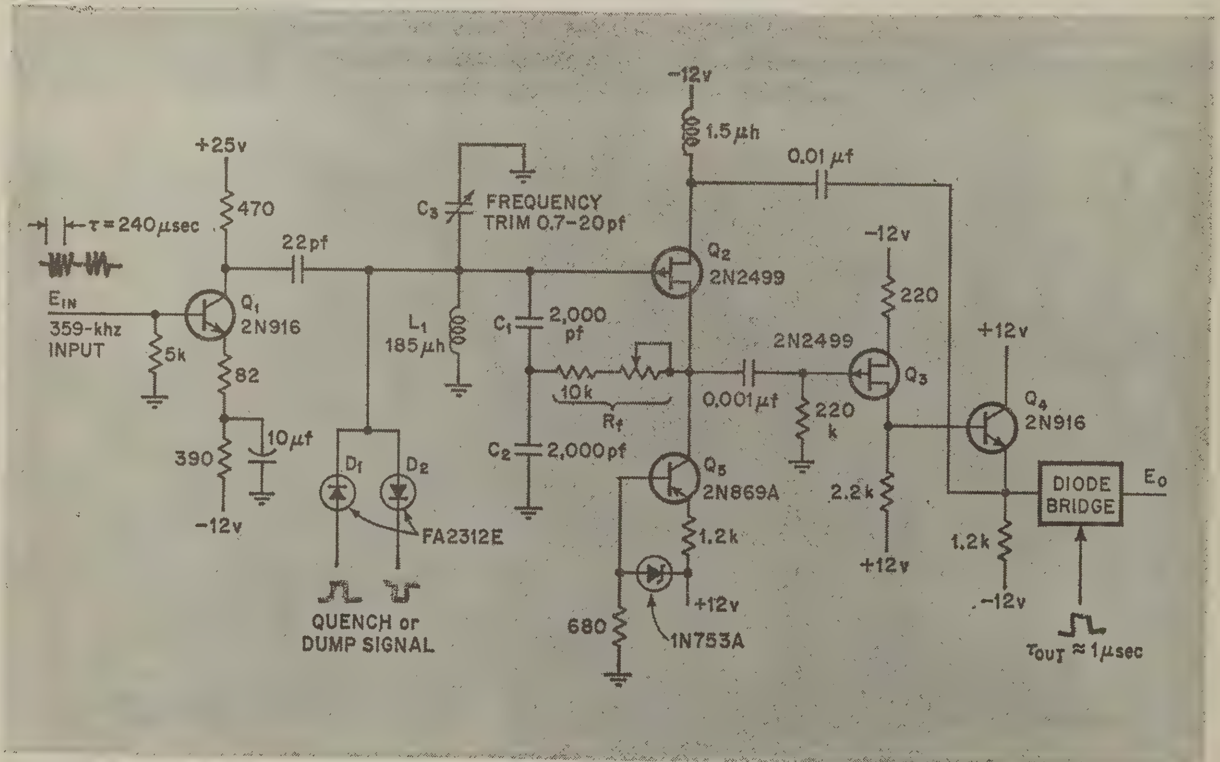
Incoming channels are multiplexed and fed into the input-buffer stage formed by transistor Q_1. The 359-kilohertz center frequency is derived from the local oscillator of a preceding mixer stage. Integration is performed in a high-Q tank circuit, which provides loaded Q's greater than 3,000. The tones are sequentially analyzed by the filter, whose characteristic is a (sine x)/x frequency response, such that only one tone, the tone tuned to the center frequency, f_o, provides a positive integral during the integration period. All other frequencies fall into the nulls of the frequency response. Thus, by controlling the frequency of the mixer, each channel's tone can be sequentially analyzed.

The multiplier uses field effect transistors to provide high impedances at the gate and source of Q_2. Q_2 provides controlled positive feedback so that Q's of 200 can be multiplied to 5,000.

As the signal is fed through the input buffer, the tank circuit, consisting of capacitors C_1, C_2, and C_3, and inductor L_1, integrates and stores the p-m signal. The stored signal becomes the bandpass audio tone with an amplitude proportional to the Q of the tank circuit. The audio signal is passed through the output-buffer stages, comprising Q_3 and Q_4, where the signal is then read out by a gated-diode bridge.

After readout, the information is erased from the tank circuit by activating the two diodes, D_1 and D_2, which de-energize the circuit with a low-impedance path to ground. The Q-multiplier is then ready to accept the next tone burst.

The Q of the multiplier is adjusted by R_f so that after the integration interval is over, the tank rings out flat over the storage interval. When the integration interval and the storage interval are selected equal to 240 microseconds, the error in integration or storage will be less than 0.5 db.



Integrated and dump. The gated Q-multiplier performs three functions: integration, storage, and filtering. The circuit operates at a center frequency of 359 khz and can generate loaded Q's from 200 to 5,000. The Q-multiplier has a (sine x)/x frequency response and generates a positive integral only for the tuned channel.

D-c-to-d-c converter offers positive or negative bias

By Gerald Olson

Denver, Colorado

For simplicity, compactness, and low cost, one of the best approaches to the design of d-c-to-d-c converters is a design using a complementary emitter follower. And with a slight rearrangement of the components, the same circuit can be made to supply a negative voltage from a positive supply.

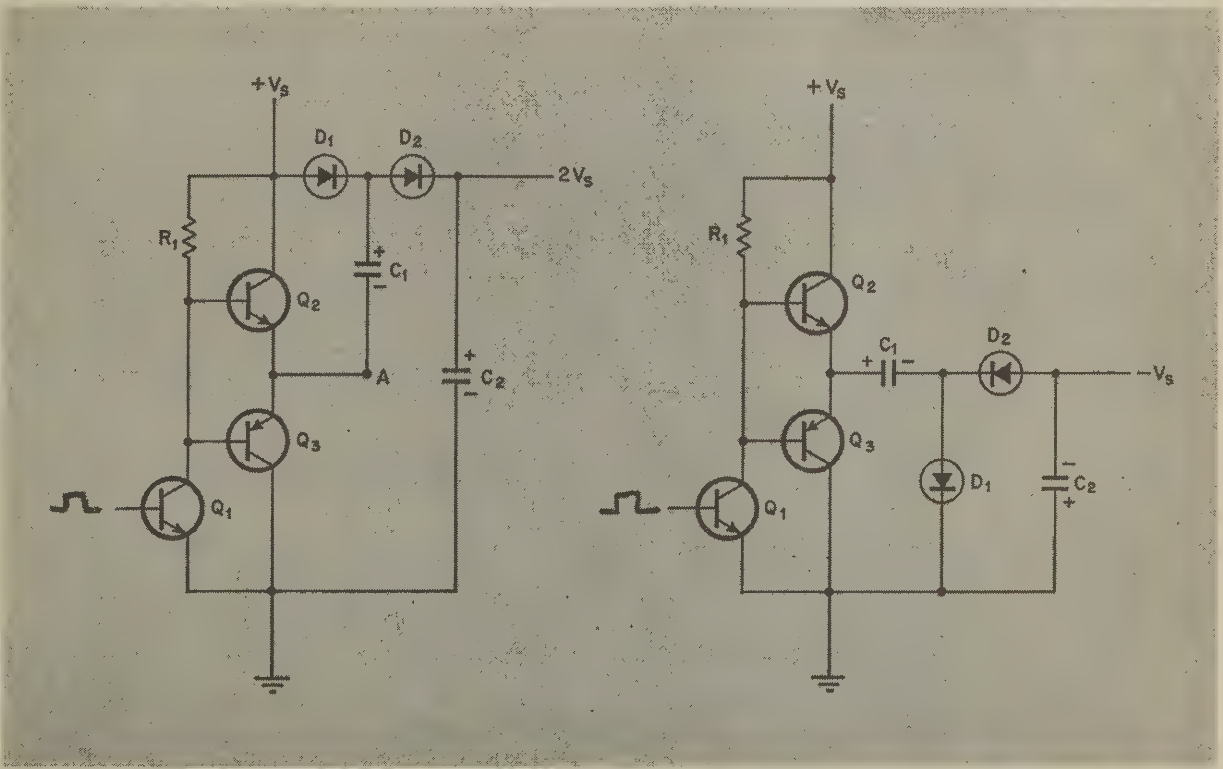
The circuit at the left shows the basic configuration of a voltage doubler, but can be easily extended to provide other multiples. Transistors Q_2 and Q_3 form the complementary emitter follower driven by the input transistor, Q_1. Q_1 is turned alternately on and off by a positive input pulse.

Before the arrival of a pulse, the transistors are off, and point A is at ground potential. The capacitor, C_1, charges to the supply voltage, V_s. When a positive pulse arrives at the input, Q_1 turns on, and drives Q_2 and Q_3 into conduction. The potential at point A rises to the supply voltage placing the circuit with the supply voltage and the capacitor, C_1, in series. The output capacitor, thereupon, charges to twice the supply voltage through the diode, D_2. The diode, D_1, prevents Q_2 from discharging C_1.

The circuit at the right contains the same components, slightly rearranged. A positive pulse turns on Q_1 which turns on Q_2 and Q_3. Capacitor C_1 charges to the supply voltage, V_s, through the circuit containing diode D_1. When the pulse terminates, Q_1 shuts off, which shuts off the complementary emitter follower, Q_2-Q_3. The charge on C_1 is then transferred to C_2 to produce the negative of the supply voltage at the output.

These transistor d-c-to-d-c converters are as efficient as the transformer types, but have the added advantage that they contain no magnetic circuits whose magnetic fields might interfere with other circuits in the vicinity. The transistor circuits also lend themselves to fabrication as integrated circuits.

Where moderate currents are involved, the frequency of operation could be high as long as satisfactory transistors and diodes can be fabricated. With high frequencies, the capacitors can possibly be made small enough so as to be also part of the IC. Such a package could be useful as a source of bias for varicap tuners.



Complementary. The complementary emitter follower (left) charges the output capacitor to twice the supply voltage, while the other one charges the capacitor to the negative of the supply. The circuits are as efficient as transformer-type converter circuits, and with smaller capacitors, can work to high frequencies.

Comparator increases rate meter's response

By Donald Wasserman and Glenn Parker

Perkin-Elmer Corp., Norwalk, Conn.

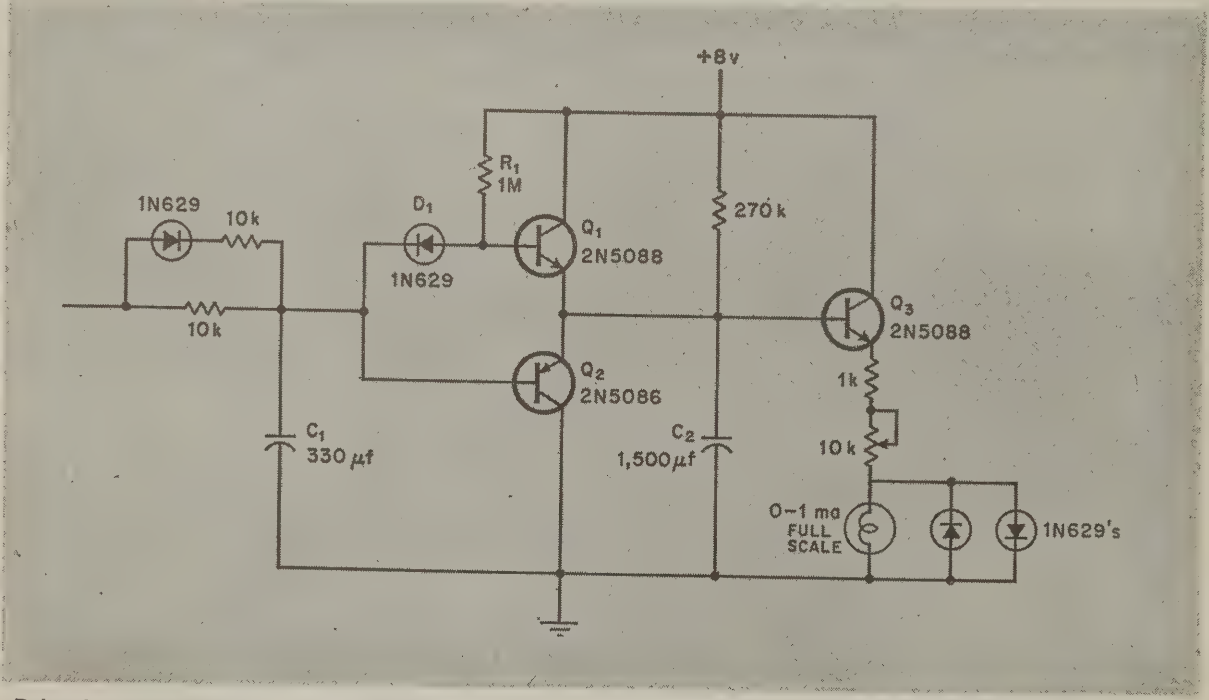
Some low-frequency rate meters, such as those used for pulse counting, produce an output voltage proportional to the repetition rate of an input pulse train. This proportional output may interfere with a reading if ripple is associated with the pulses. A larger time constant to smooth the ripple results in poorer response time. Adding a simple comparator circuit to the integrator improves the measurement response time of the rate meter.

Transistors Q_1 and Q_2 make up the comparator, comparing the voltage developed across C_1 to that across C_2. The voltage developed across C_1 results from the pulses arriving at the input from the output of the preceding monostable multivibrator stage (not shown here). Essentially, capacitor C_1 responds fast, while C_2 filters the ripple.

If, for example, the input repetition rate should slow down, the voltage across C_1 will decrease, turning Q_2 on. Capacitor C_2 then discharges quickly through the low-impedance path of Q_2 to ground, until the voltage across C_2 is about equal to that of C_1. The output emitter follower, Q_3, follows the change in voltage across C_2 and delivers the meter readout.

Similarly, if the input rate should speed up, the voltage on C_1 would rise, turning Q_1 on, providing charging current to capacitor C_2 through the low-impedance path of Q_1, until the voltage across C_2 is again about equal to that on C_1.

Diode D_1 helps reduce the voltage-comparison dead band between C_1 and C_2. And since high-beta transistors are used, R_1 can be made large enough to render negligible the current it contributes to C_1 through D_1.



Balancing act. If the input rate should speed up or slow down, capacitor C_2 will follow C_1's voltage by charging or discharging rapidly through Q_1 and Q_2. The output emitter follower delivers a voltage proportional to the repetition rate of the input pulse train.

Monostable protected against 60-hertz pickup

By Vladimir Bicik

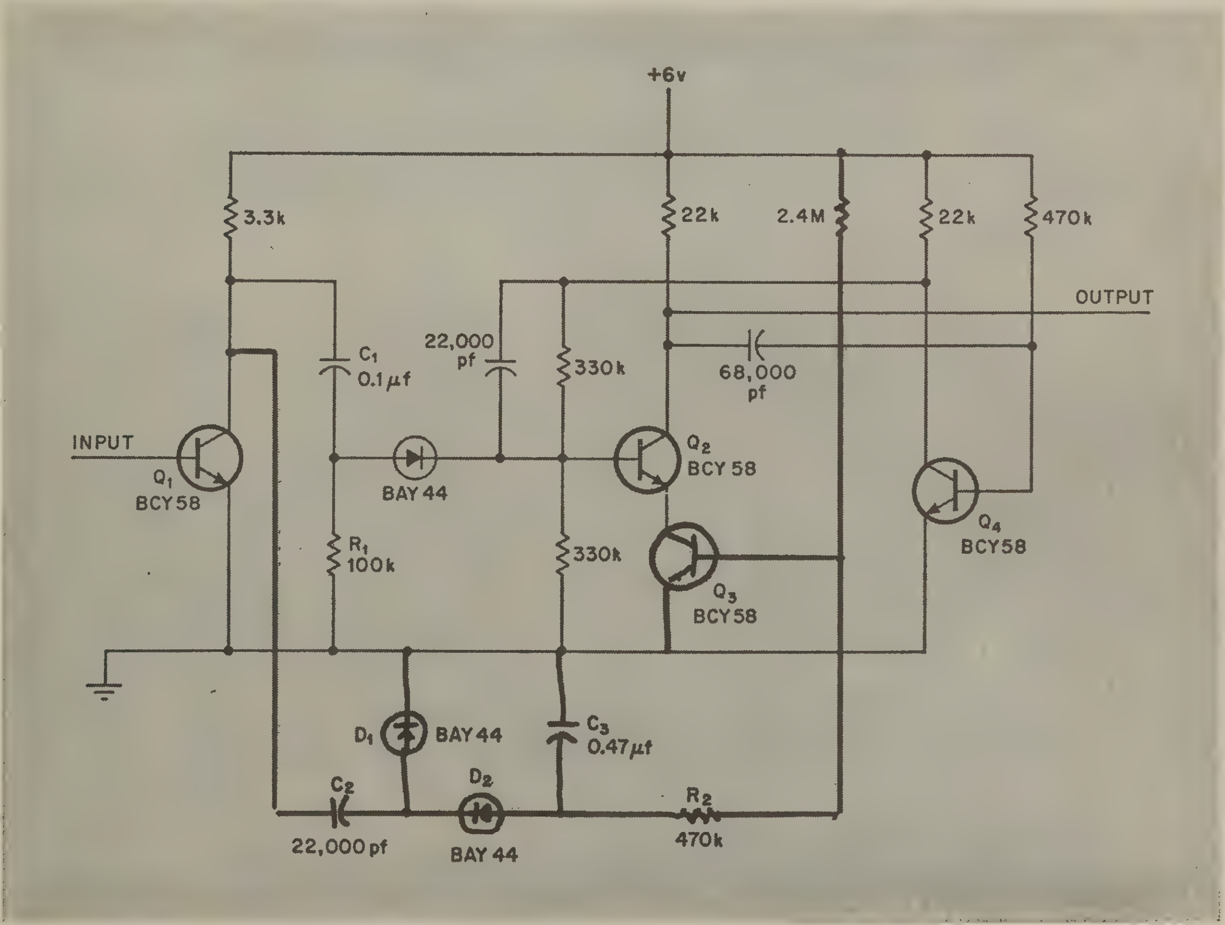
Prague, Czechoslovakia

Often, a 60-hertz pickup from faulty system grounding leads to falsely triggered monostable multivibrators. Building an extra transistor and a frequency-to-voltage converter into the circuit protects against such events. These additions effectively lock out frequencies higher than the triggering signal.

One important application—medical electronics—relies on impulses from the monostable to indicate heart activity. Here, the monostable output inhibits a cardiac pacemaker when the heart is operating on its own. Interference could be interpreted by the pacemaker as a sign of heart action and turn off when it is actually needed.

Transistor Q_1 detects and amplifies signals arriving from the heart. The signals are differentiated by R_1-C_1 and fed to the monostable Q_2-Q_4.

The highest frequency signal from the heart will be in the range of 12 to 150 beats per minute or 2 to 2.5 hertz. A voltage-doubler circuit, comprising C_2, C_3, D_1, and D_2, senses the input pulses and converts them to a voltage, which develops across capacitor C_3. As long as the frequency is in the range of 2 to 2.5 hz, little accumulated voltage appears across C_3, since the voltage has time to discharge through R_2 before the next pulse appears. Should a 60-hz signal be picked up and amplified by Q_1, this increased frequency would begin to charge C_3 and drive its voltage more and more negative with respect to ground. The capacitor will not be capable of discharging through R_2, and thus Q_3 will quickly cutoff. When Q_3 cuts off, the monostable circuit becomes inhibited, signaling the pacemaker to begin functioning.



Heart action. This monostable is inhibited from producing output pulses should 60-hertz interference be picked up by input amplifier Q_1. The voltage doubler (shown in red) would charge capacitor C_3 until its negative voltage cuts off Q_3. When Q_3 shuts off, the monostable circuit, Q_2-Q_4, cuts off.

One-shot generates wide range of periods

By Seymour Bell

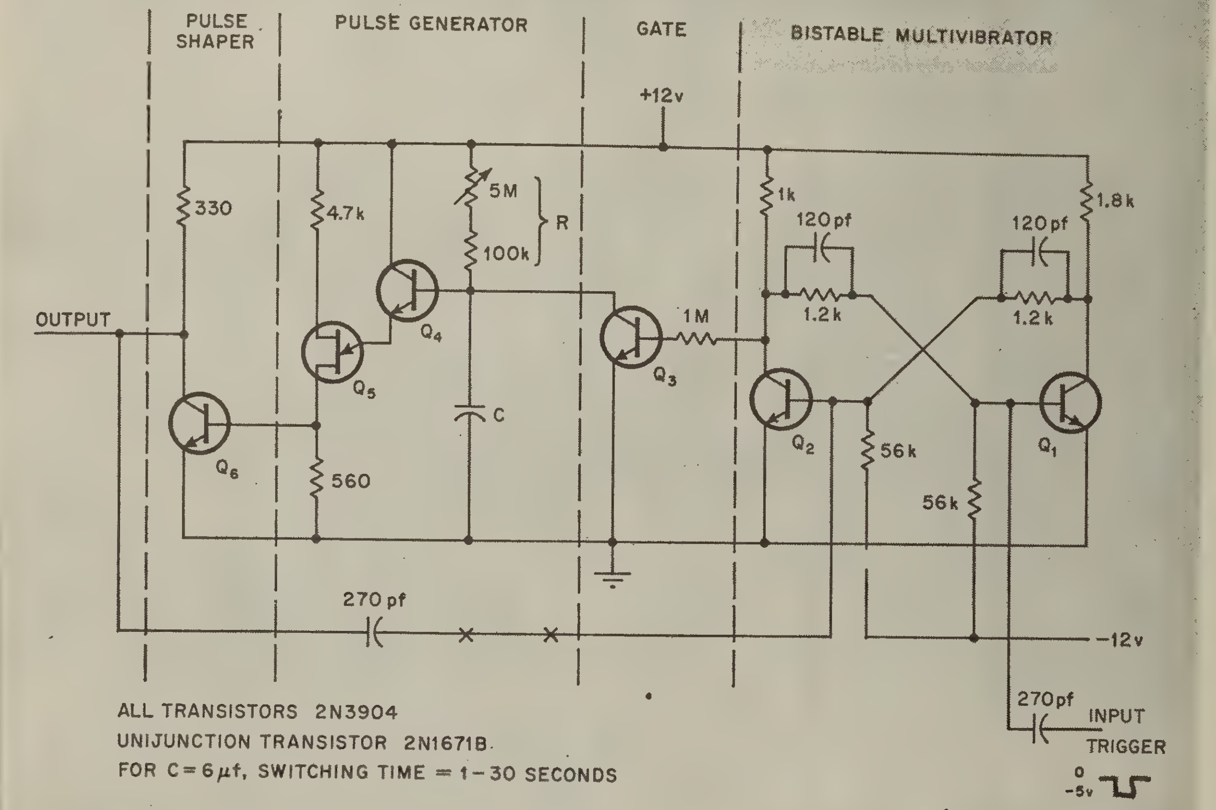
University of Michigan, Ann Arbor

Gating a pulse generator with a bistable multivibrator produces a large variation in the time constants, and thus in the pulse width, of a monostable multivibrator. The combined circuit generates pulse widths of less than one tenth to greater than 100 seconds.

Essentially, the circuit consists of the bistable multivibrator, a transistor gate, the pulse generator, and a pulse shaper. In the bistable's normal state, transistor Q_1 is on and Q_2 off. A positive voltage thus appears at the base of the transistor gate, Q_3, forcing it on. While Q_3 is on, the pulse generator's timing capacitor C short circuits keeping the pulse generator off.

A negative trigger pulse applied to the input of the bistable multivibrator starts the action of the monostable circuit. Transistor Q_1 switches off, turning Q_2 on, which, in turn, switches Q_3 off. When Q_3 turns off, the timing capacitor starts charging through the resistor network, R, towards the 12-volt supply. The unijunction transistor fires when its critical voltage is reached. The pulse out of the unijunction is shaped by Q_6 and fed back to the bistable, which then returns to its normal state and awaits the next trigger pulse. The action of the bistable shuts off the pulse generator.

The pulse generator determines the time constant of the overall circuit. The upper limit of the time constant is determined by the combined leakage of Q_3 and timing capacitor C, and by the gain of Q_4. The time constant can be multiplied by a factor of 2 for each toggling flip-flop inserted in series between the points marked X—the output of the pulse shaper and the input to the bistable.



ALL TRANSISTORS 2N3904
UNIJUNCTION TRANSISTOR 2N1671B
FOR C = 6 μf, SWITCHING TIME = 1–30 SECONDS

Variable. The wide range of time constants from the monostable circuit results from the longer period provided by the unijunction pulse generator. A negative input trigger flips the bistable circuit, which turns on the pulse generator. The output pulse is then fed back and turns off the bistable.

'Make-before-break' mode improves FET switch

By Leonard F. Halio
Digital Equipment Corp., Maynard, Mass.

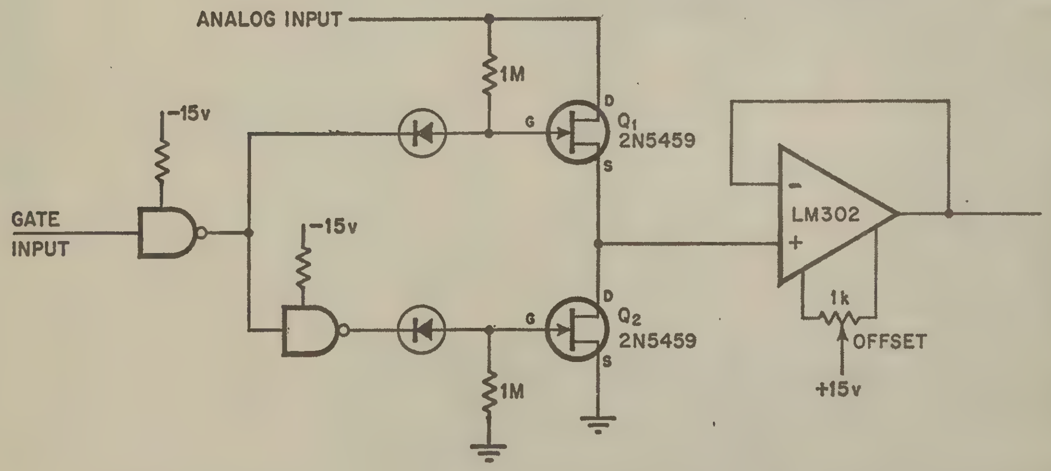
When field effect transistors are used to switch analog signals spikes often are transmitted with the signals. And a finite resistance associated with the FET varies with temperature changes, introducing further inaccuracies. These problems can be overcome with a circuit scheme using two FET's operating in a make-before-break mode. Here, one of the transistors is switched on prior to gating the analog signal. This provides a low-impedance path to ground which minimizes the spikes.

Since the channel resistance of the FET and its input capacitance are inversely proportional, merely attempting to lower the channel resistance will not eliminate the problem. Input capacitance would increase when channel resistance is decreased, allowing the gating signal to be coupled through the FET's channel and into the analog system.

In the circuit configuration, a positive gating signal turns on transistor Q_1 while Q_2 remains off, thus allowing the analog signal to be transmitted to the output via the operational amplifier LM 302. Since Q_1's channel resistance is in series with the 1,000-megohm input impedance of the operational amplifier, variations in the smaller channel resistance over wide temperature ranges can be ignored.

When the analog switch is opened by a negative-gating signal, the time constants of the associated drivers of Q_1 and Q_2 are adjusted to allow Q_2 to turn on before Q_1 turns off—hence, the make-before-break scheme. Any spike coupled through Q_2 sees a low-impedance path through Q_1, effectively reducing the spike to a negligible value.

This process is repeated when Q_1 turns on and Q_2 turns off. The coupling signal will see a momentary low-impedance path through Q_2 to ground, reducing the spike to a negligible value.



Low impedance. The two FET's acting as a make-before-break switch help reduce troublesome spikes from being gated with signals in an analog switch. The time constants of the associated drives of Q_1 and Q_2 are adjusted to allow Q_2 to turn on before Q_1 goes off, and vice versa, minimizing the gating transients.

Short-circuit protection for voltage regulators

By W. Granter

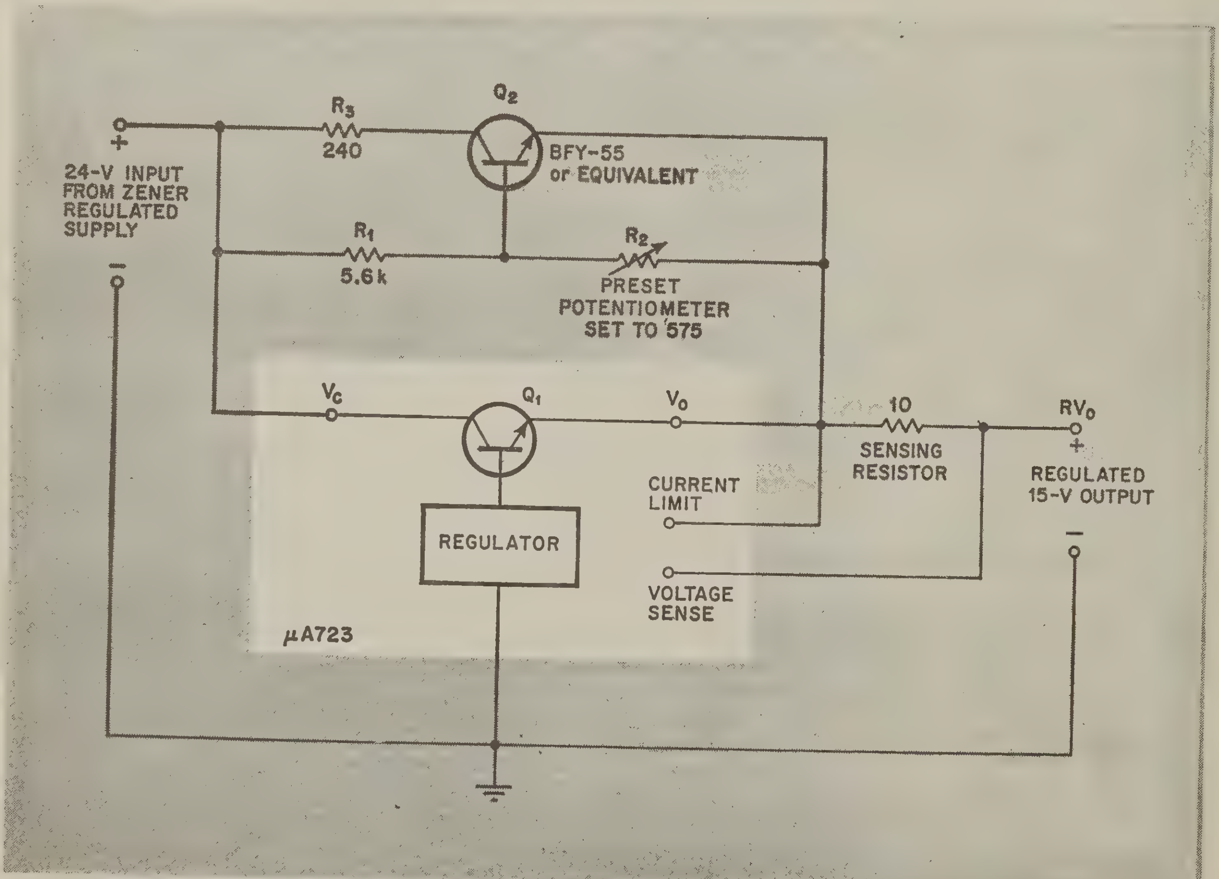
Central Research Laboratories, Shortland, Australia

A short circuit occurring at a voltage regulator's output could destroy the regulator's series pass transistor. But if a transistor network is added across the series pass transistor terminals the increased current due to a short circuit will be partially drained off by the added transistor. This would hold the power dissipation of the series transistor within acceptable limits.

A typical voltage regulator, the μA 723, provides a 15-volt output with a load current of 40 milliamperes. If the load terminals of the device (RV_o and ground) are short-circuited, the output voltage adds to the normal voltage drop across the series pass transistor, Q_1, in the output stage of the regulator. The new 24-volt supply voltage combined with the 40-ma current increases power dissipation to 960 milliwatts, overloading the regulator by 160 mw.

The modified circuit works as follows. During normal operation, V_o is approximately equal to 15 volts. Transistor Q_2 is biased off by an appropriate selection of values for R_1 and R_2 and has a standby current drain of 10 ma. When RV_o is short-circuited to ground, the voltage across the series pass transistor (V_c to V_o) rises, causing the voltage across R_2 to rise to a voltage exceeding the 0.6-volt turn-on value for Q_2. Current then is drawn through R_3, reducing the load carried by Q_1. R_3 is selected to allow Q_1 to draw 10 ma while 85 ma flows through Q_2 and R_3. Now the power rating of the series pass transistor is not exceeded and the voltage regulator has a built-in short-circuit protection.

The modification protects any series pass transistor when the values for the resistors and the current limit for Q_2 are calculated to share the load with the transistor to be protected.



Series bypass. An additional transistor circuit connected across the series pass transistor of a voltage regulator protects the series transistor from overloading if a short circuit occurs across the regulator's output. Transistor Q_2 is biased into conduction during a short circuit, draining off the extra current.

Two op amps simplify design of oscillator

By Dennis J. Knowlton

University of Wyoming, Laramie

A voltage-controlled oscillator, of the type commonly used in analog-to-digital converters, can be quickly built with readily available components. The frequency, which is linearly proportional to an input voltage, varies from 0 to 1 kilohertz over an input voltage range from 0 to 5 volts.

The oscillator comprises three parts: an integrator, a voltage detector (Schmitt trigger), and a reference voltage network. The integrator, built with operational amplifier A_1, converts a positive input voltage to a negative-going ramp at its output terminal. Op amp A_2 acts as a Schmitt trigger with thresholds—determined by resistors R_4 and R_5, and by the voltage reference attached to R_4—of —2 volts and —7 volts.

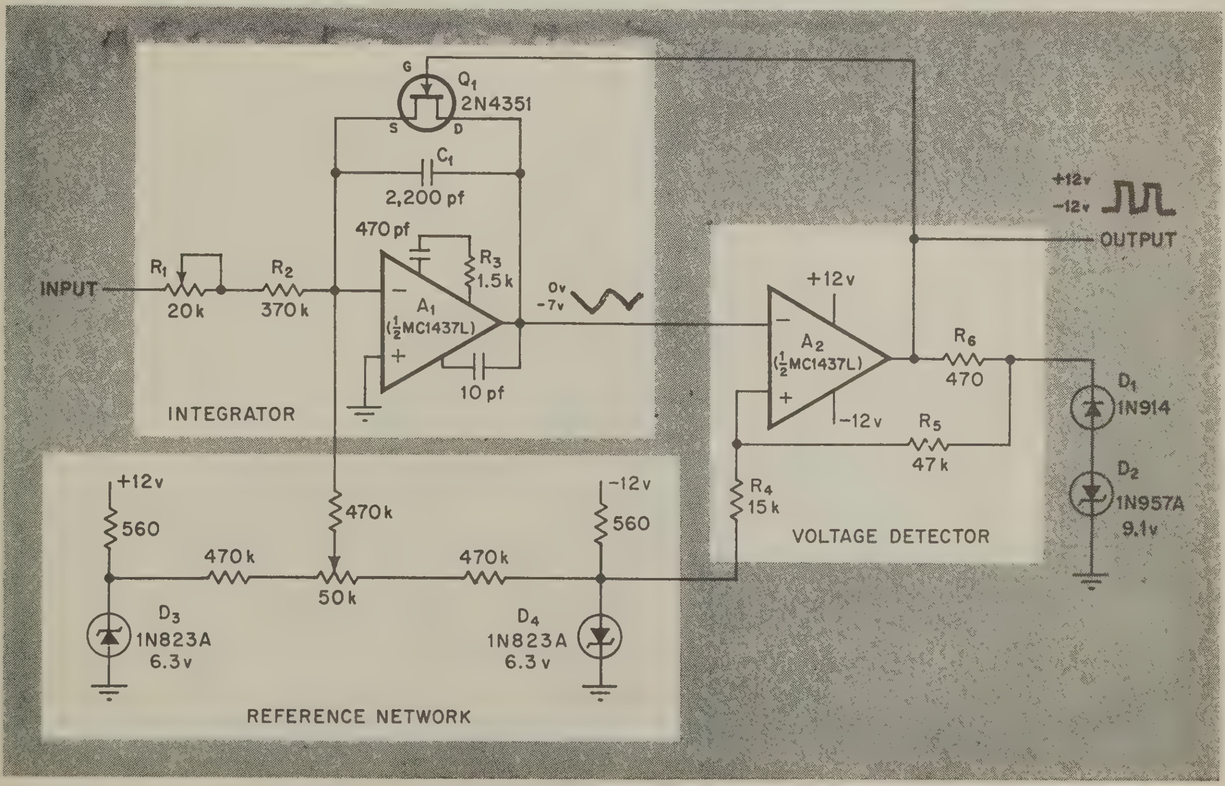
The output of the integrator is initially at 0 volt. The Schmitt trigger's output sits at —12 volts. When a positive voltage is received at the input, the integrator charges negatively until it reaches —7 volts, whereupon the Schmitt trigger fires and produces an output voltage of 12 volts.

The 12-volt output is fed to the gate of field effect transistor Q_1 which immediately turns on. This action causes the integrating capacitor, C_1, to discharge and clamp the integrator's input to —7 volts. The result is that the integrator now begins to deliver a positive-going ramp at its output terminal.

The integrator's output voltage continues to increase toward 0 volt until it reaches the Schmitt trigger's second firing voltage of —2 volts. At this voltage, the output of A_2 returns to —12 volts, shutting off Q_1. When the integrator's output voltage reaches 0 volt, the cycle is completed and a new cycle begins.

Diodes D_1 and D_2, and resistor R_6 stabilize the —7-volt trigger point against variations in the —12-volt supply. The reference network supplies the voltages for the trigger points and provides a common input bias compensation for the op amps.

The oscillator remains linear to within 0.1% over a frequency range of 0 to 1 khz. The output frequency remains stable to within 0.1% for variations in the supply voltage up to ±15%.



Voltage-controlled. The frequency is linearly proportional to the input voltage. When the integrator reaches —7 volts, the detector switches to 12 volts. Q_1 turns on, discharging C_1 and the integrator begins to charge toward 0. At —2 volts, the detector again fires and produces a —12 volt output.

Unijunction device eliminates contact bounce

By Carl Brogado

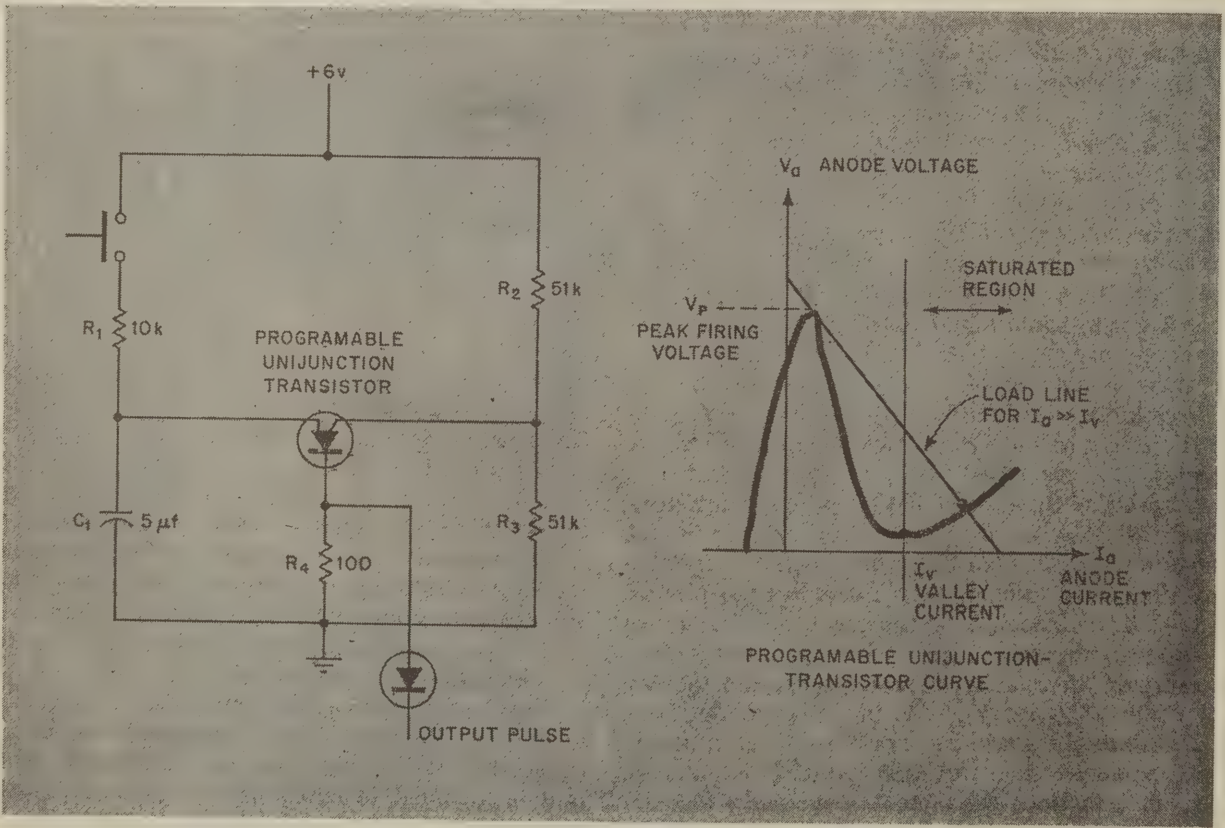
Technetics, Inc., Boulder, Colo.

A simple way to eliminate the contact bounce from mechanical switches relies on a programable unijunction transistor to generate a clean pulse. The unijunction transistor can be programed from whatever supply voltage is desired, whereas other circuits containing integrated circuits are restricted to the IC's supply whose voltage must be filtered to prevent accidental triggering from transients in the system.

The unijunction's firing voltage is set for 3 volts by the voltage divider, comprising R_2 and R_3. When the switch is depressed, C_1 begins to charge toward the supply voltage through R_1. The voltage divider allows the voltage on C_1 to reach the transistor's peak firing voltage, at which point the transistor discharges the capacitor, producing a positive pulse at R_4. The charging rate of the pulse is determined by the values of resistor R_1 and capacitor C_1.

The value of R_1 is chosen so that the charge current, I_a, is much greater than the valley current, I_v, for the transistor. Thus, the transistor will remain in the saturation region until the pushbutton switch is released.

This scheme has proven to be completely immune from any contact bounce produced by the switch.



Clean and free. With a programable unijunction transistor, clean pulses can be generated free of switch-contact bounce with whatever supply voltage is being used. When C_1 charges to the transistor's peak firing voltage, the transistor discharges the capacitor and generates a pulse at R_4.

Bridge circuit relies on common ground

By Gilbert Bank

Westinghouse Ocean Research Lab., San Diego, Calif.

A bridge circuit is frequently used at the output stage of an amplifier when large bipolar output voltage swings are generated. While maintaining the same drive level to the load, the bridge circuit halves the requirements on the V_{ceo} breakdown characteristics of the output transistors. Most bridge circuits require the load to float, but this circuit overcomes this disadvantage by using a common ground for both the input and output. However, it does require a floating power supply.

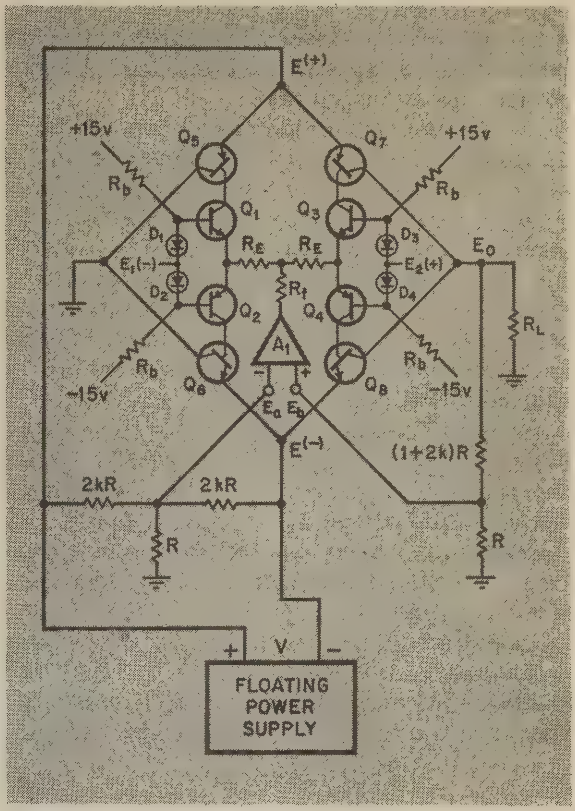
The input transistors, Q_1 to Q_4, drive the bridge output transistors, Q_5 to Q_8. Resistors, R_b, and diodes, D_1 to D_4, bias the circuit into class AB operation, thus preventing crossover distortion.

The positive and negative inputs are E_2 and E_1, respectively, and the output is taken at E_0. Either input may be grounded or driven. The circuit can be treated as a low-gain differential amplifier. If E_1 is grounded and E_2 is driven positively, Q_3 and Q_2 are forward-biased, and they in turn, drive Q_7 and Q_6 into conduction.

Due to the beta differences in the transistors, the voltage drops across Q_6 and Q_7 will not be equal. This results in an unequal power dissipation. The voltage differences are sensed by appropriate divider networks and are brought into the common-mode range of the amplifier at E_a and E_b. Amplifier, A_1, senses this difference and supplies a current through R_f into the resistors R_e in such a way as to correct any unbalances in the opposite legs of the bridge.

Although not shown here for simplicity sake, resistors should be inserted in the collector circuits of transistors, Q_1 to Q_4, and in the emitter circuits of transistors, Q_5 to Q_8.

Because the bridge is automatically balanced, it is not necessary to use matched-transistor complements for Q_5 and Q_6, and Q_7 and Q_8. Good performance can be obtained using silicon npn transistors and germanium pnp transistors.



Good drive. The bridge circuit with common input and output grounds, can be used at the output of amplifiers to deliver large bipolar voltages to loads.

Divider splits frequency into any ratio from 1 to 99

By Ken Erickson

Interstate Electronics Corp., Anaheim, Calif.

This programable pulse-frequency divider breaks down frequency into any submultiple with ratios from 1 to 99. Two thumbwheel switches provide the programed division ratio to a decade-counter integrated circuit. Frequencies exceeding 10 megahertz can be divided by the circuit.

The counter easily expands to form several decade stages with proportionately larger division ratios.

A two-stage synchronous counter which generates the new frequency, is made from two decade counters of four bits each. As an example of how the division ratio is accomplished, assume a ratio of 3 is desired. Switch S_1 is set at 3 and S_2 at 0. This ratio is internally converted by the switches to a 9's complement binary code which makes up the preset data for the decade counter. Thus the 9's complement of 03 is obtained by subtracting each digit from 9 to get 96. The binary-coded decimal equivalent of 96 is generated at the output terminals of the thumbwheel switches. Outputs from switch S_1 appear on lines 4 and 2, while S_2 outputs are on lines 1 and 8.

The decade counter starts at a count of 96. Gate 2's input from T_c is enabled, because the T_c output of the counter is a logic 1 when the counter is at its maximum count of 9 and also during a carry when more than one stage is used. However, the input to gate 2 from Q_3 of the units part of the decade counter is inhibited—Q_3's output being a logic 1 only on the counts of 8 and 9. Therefore, no pulse is transmitted through gate 2 during the counts of 96 and 97. Each input pulse steps up the counter by one, but no pulse appears at gate 2's output until a count of 98 is reached; then a logic 1 appears both at the T_c output and the Q_3 output of the counter. The one-shot multivibrator is triggered and delivers a pulse to the output via the pulse transformer, T_1, which serves to isolate grounds.

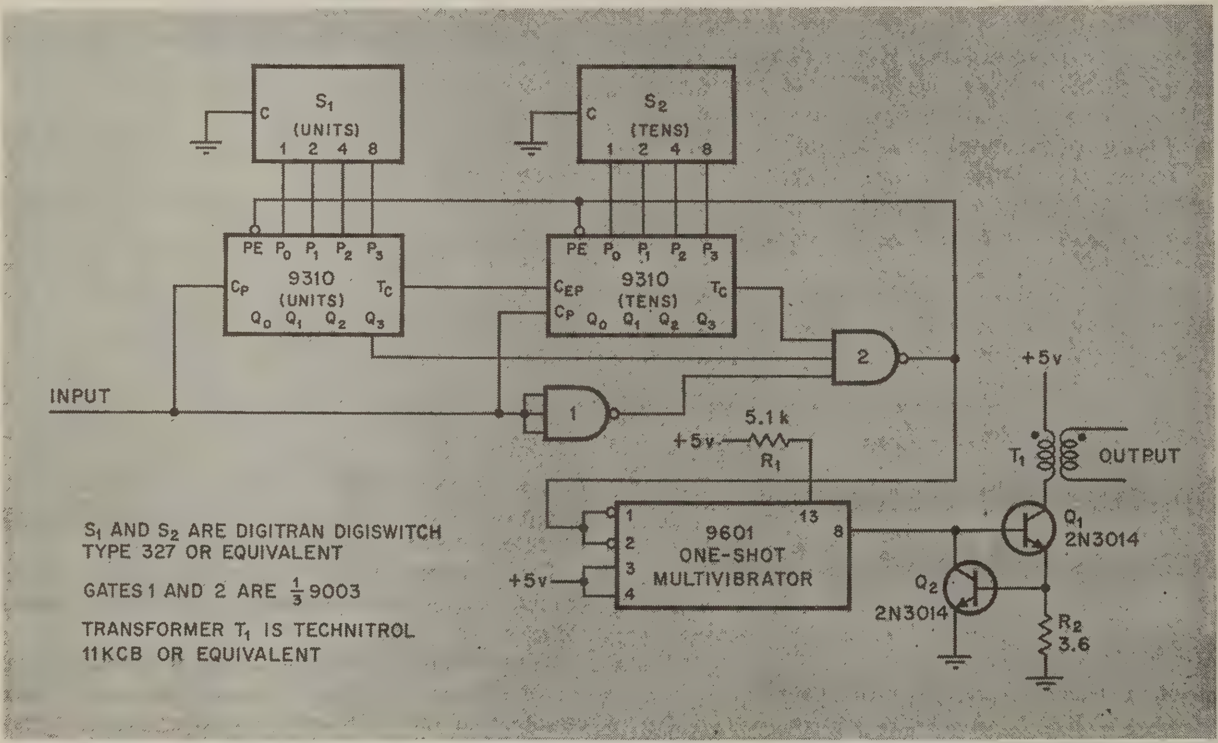
On the arrival of the next input pulse, a carry is generated at both T_c outputs of the counter enabling the counter's PE inputs and resetting the count to the original preset coded input. As shown below, the decoded output is a logic 1 every third count giving a division ratio of three.

clock no.	count	decoded output logic level
1	96	0
2	97	0
3	98	1
4	96	0
5	97	0
6	98	1
7	96	0
8	97	0
9	98	1

A terminal count of 98 is decoded instead of 99 to allow for the one clock cycle required for the synchronous preset of the two decade counters.

Gate 1 inverts the input signal. The inverted signal feeds gate 2 for the purpose of implementing the special case of divide-by-one. For this particular division ratio, the counter's terminal count and the preset code are the same. This means that the outputs of the counters never change state.

The one-shot multivibrator provides the pulses needed to drive the pulse transformer. With the value of R_1, the pulse width is typically 45 nanoseconds. Transistor Q_2 and resistor R_2 are used to limit the current of Q_1 in case of an inadvertent short-circuit across the transformer's secondary winding.



S1 AND S2 ARE DIGITRAN DIGISWITCH TYPE 327 OR EQUIVALENT

GATES 1 AND 2 ARE $\frac{1}{3}$ 9003

TRANSFORMER T1 IS TECHNITROL 11KCB OR EQUIVALENT

Choice of ratio. Any desired division ratio of input clock pulses can be obtained by setting the switches, S_1 and S_2 to the ratio. The preset data is supplied to the decade counter as a nine's complement code. The decade counter counts from the preset value to a count of 98, whereupon it returns to its preset value.

Negative impedance stabilizes motor's speed

By Sam Ben-Yaakov

University of California, Los Angeles

A small d-c motor is subject to speed variations with load, even when driven by a constant voltage source. But a negative impedance inserted in series with the motor can hold speed variations under load to within 2% for a given control voltage setting over a long time period.

The electromotive force developed by the motor is linearly proportional to the motor's speed:

$$\text{EMF} = Kn$$

where K is a constant and n is the motor's speed. If the motor with internal resistance R_i is driven by a voltage source V_s with an internal resistance R_s, it will develop a speed:

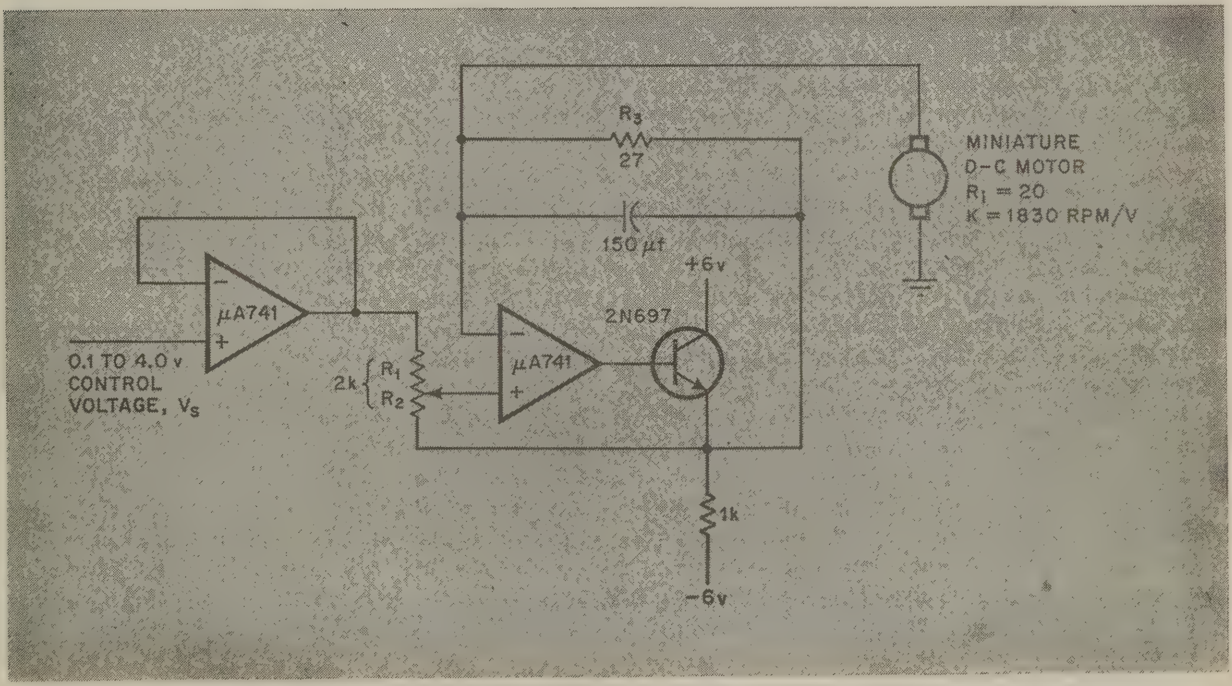
$$n = \frac{\text{EMF}}{K} = \frac{V_s - i\,(R_s + R_i)}{K}$$

where i is the current through the motor. If R_s is made negative and equal in magnitude to R_i, then the speed equation reduces to V_s/K. Thus the motor's speed is a function of V_s and is independent of the load.

The negative resistance is achieved through a negative impedance converter, an operational amplifier connected with both positive and negative feedback. The source resistance presented to the motor, which is placed between the negative input of the op amp and ground, is controlled by the resistance ratio $-R_1R_3/R_2$ and can be adjusted to approach the value of R_i by the 2-kilohm R_1–R_2 potentiometer.

Although the nominal voltage of the motor is 6 volts, the control voltage can be adjusted to provide a wide range of motor speeds.

The capacitor prevents the circuit from oscillating, and the transistor generates the needed drive to the motor.



Negative impedance. The equivalent resistance of the motor's driving source is made equal to the negative of the motor's internal resistance thereby rendering the motor's speed independent of load variations. The negative impedance is measured at the op amp's negative terminal with respect to ground.

Signal detector operates from 5-volt supply

By D.K. Smith

General Dynamics Corp., San Diego, Calif.

A unijunction transistor circuit that detects the presence or absence of signals can be easily used with a digital logic network. This feature is made possible by its ability to operate from a 5-volt supply and its low power consumption—18 milliwatts. When a signal is present, the output across the load rises to the supply voltage level, while in the absence of a signal the output falls to ground.

The timing circuit consists of the unijunction transistor Q_2, timing components R_t and C_t, and the silicon controlled rectifier Q_3 and its associated resistors. The unijunction transistor normally is free-running at a frequency determined by R_t and C_t. The SCR thus is continually triggered and turned on through the load. The output remains at ground, indicating the absence of an input signal.

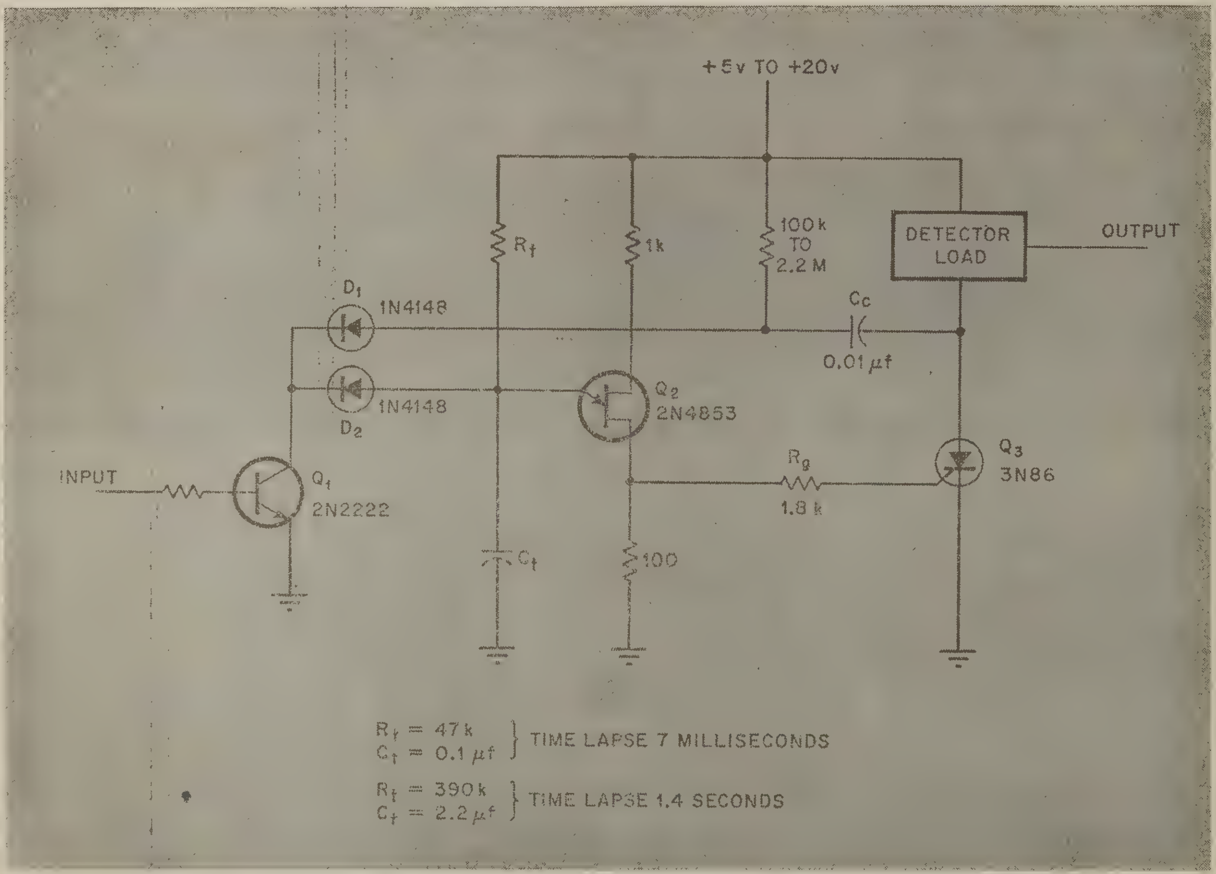
A signal arriving at the input, turns on transistor Q_1. The unijunction transistor's emitter is grounded, thus inhibiting the timing circuit. In addition, Q_1 transmits a negative-going pulse through diode D_1 and the capacitor C_c to Q_3's anode, turning off Q_3. The voltage at the detector load's output rises, indicating that an input signal is present.

When the input signal terminates, the timing circuit is again freed, but only after a time lapse determined by the period of the unijunction circuit. If another input pulse arrives before Q_2 is triggered, the time lapse is restarted.

The holding time may be varied from a few microseconds to a few seconds.

The detector load is current-sinking logic which provides the holding current for the SCR. The purpose of the resistor R_g is to reduce the holding current requirement for the SCR.

The circuit has been operated over a temperature range of −25°C to +75°C.



Knowing when. When a signal is present at the input, Q_1 turns on, grounding the unijunction transistor's emitter and inhibiting the timing circuit. In addition, a negative-going signal is transmitted to Q_3's anode, turning off the SCR. The voltage across the load rises, indicating the presence of an input signal.

Inverted-mode transistors give chopper low offset

By R.C. Scheerer and J. Logis

Westinghouse Defense and Space Center, Wash., D.C.

A balanced chopper transistor modulator using two npn and two pnp transistors connected in the inverted mode instead of the standard transistor configuration give a much lower offset voltage. Furthermore, the need for matched transistor pairs is eliminated, while only one secondary winding is required in the transformer.

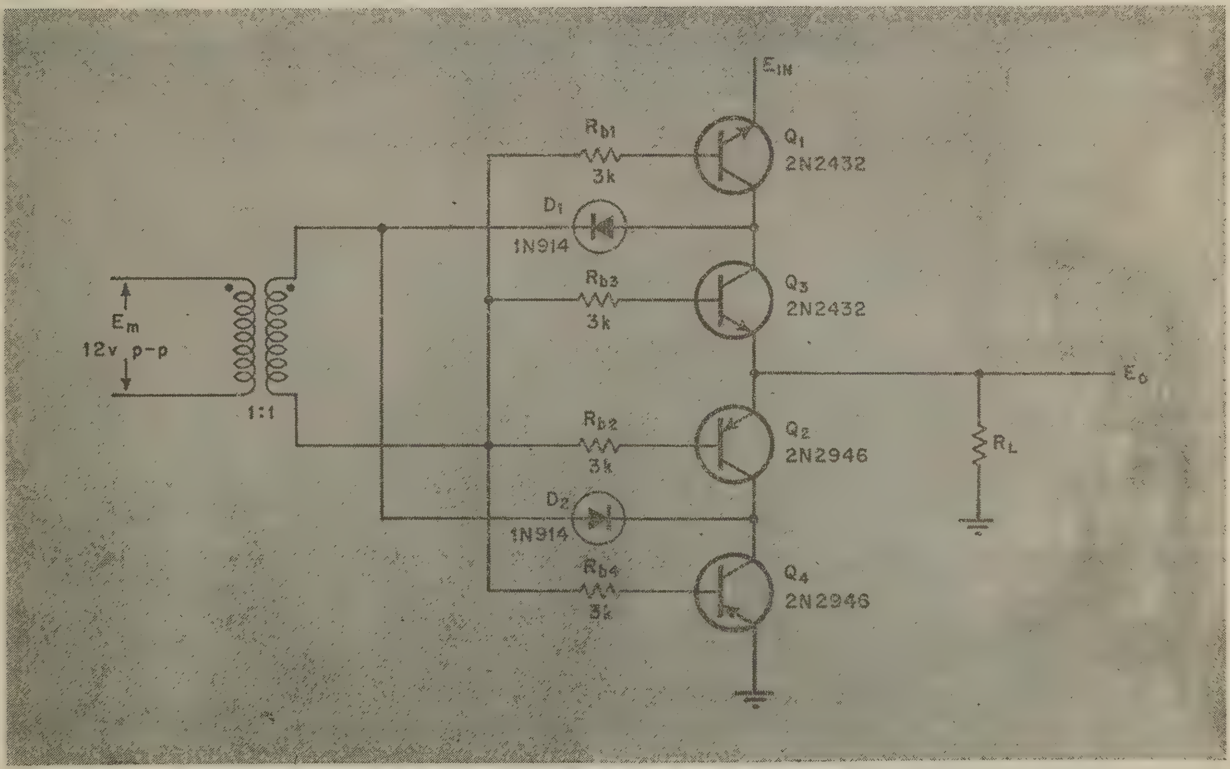
The circuit is useful in chopper-stabilizing amplifiers, frequency-modulated oscillators, synchronous modulating/demodulating circuits and regulated a-c power supply design.

Most other designs require matched transistors so that the collector-emitter saturation voltages cancel and track with temperature variations. In this modulator, the transistors connected in the inverted mode have a saturation voltage of 2 to 4 millivolts and offset voltages are usually as much as four times less than in other designs.

On positive-half cycles of the modulating excitation voltage, E_m, the base-collector junctions of Q_2 and Q_4 are forward-biased, and these transistors conduct. Transistors Q_1 and Q_3 are reverse-biased and remain off. Current flow through the collector-base junctions of Q_1 and Q_3 is blocked by diode D_1; the output voltage thus is at ground potential. Since the chopper transistor is connected in the inverted mode, a much lower $V_{ce(sat)}$ is obtained (2 to 4 millivolts), against the 0.2 to 0.4 volts obtained for standard transistor saturation voltages.

And since the emitter-collector voltages of the conducting pair of transistors are equal but opposite in polarity and tend to cancel each other, the offset is further minimized. These voltages tend to track with temperature.

On negative-half cycles, the base-collector junctions of transistors Q_1 and Q_3 are forward-biased, thus driving the transistors into saturation. Sufficient base drive is obtained by the proper selection of resistors R_{b1} and R_{b3}. Transistors Q_2 and Q_4 are reverse-biased and remain off during the negative cycle. Current flow through the collector-base junctions of Q_2 and Q_4 is blocked by diode D_2. The voltage at the output during this interval rises to the input voltage, E_{in}.



Modulator. Chopper transistors (two npn's and two pnp's) are used in their inverted mode instead of the standard configuration to produce saturation voltages in the range of 2 to 4 millivolts, against the common saturation voltages of 0.2 to 0.4 volts in other modulator designs.

Zener in bootstrap extends amplifier's range to d-c

By Roland J. Turner

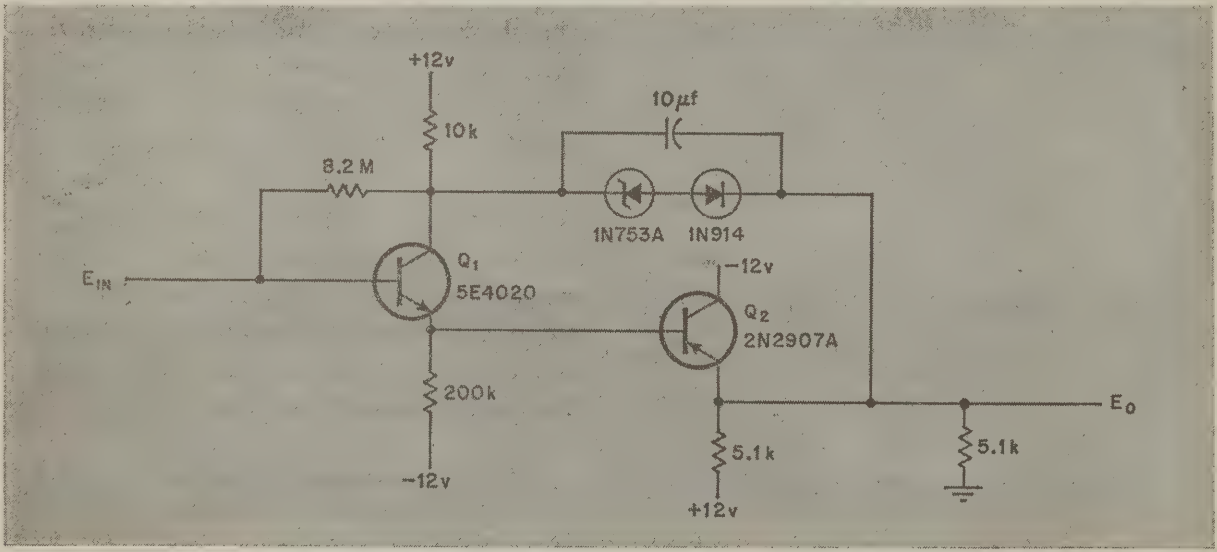
General Atronics, Philadelphia, Pa.

The input impedance of a conventional Darlington amplifier, limited to 2 megohms by the collector-to-base shunt loading of the input transistor, can be increased through a bootstrap arrangement. By placing a zener diode in the feedback circuit between the output transistor's emitter and the input transistor's collector, the input impedance is boosted to 30 megohms while input capacity is reduced from 4.5 picofarads for a non-bootstrapped stage to 0.5 pf for this circuit. And whereas other bootstrap arrangements are effective only for a-c signals, the zener diode bootstrap assures operation down to d-c signals as well.

The circuit's good low-frequency response makes it especially useful as an isolation amplifier in applications such as medical sensors and hydrophone transducers.

The Darlington circuit consists of complementary transistors which enable the output voltage to track the input over temperature variations with negligible d-c offset. As the input signal changes by some amount, V, the output, E_0, changes by KV where K is gain of the amplifier, and the input transistor's collector changes by the same amount. Thus the input resistance r_{c1} is effectively increased by $1/r_{c1}(1\text{-}K)$, with K usually being close to 1. Since the feedback capacitor represents a high reactance at low frequencies, blocking d-c, the zener diode extends the amplifier's operating range to d-c.

With super beta transistors such as the MC1556 used for the input transistor, an input resistance exceeding 100 megohms can be attained readily. These super beta transistors have a low breakdown voltage in the range of 5 to 7 volts, but by using a IN750A zener diode in the bootstrap connection, the maximum voltage that can develop across the terminals of Q_1 always is less than 5 volts (the zener breakdown voltage) even when the input signal swings are in the 10- to 100-volt region. The upper limit of dynamic range is limited only by the supply voltage and the breakdown rating of transistor Q_2.



Low frequency. The zener diode bootstrap extends the operating range of the Darlington amplifier to d-c. Input capacity is reduced to 0.5 pf from the common 5 pf. With super beta transistors, input impedances in the 100-megohm range can be achieved, while the zener diode protects the transistors from breakdown.

Two MOS FET's form transient-free linear gate

By John M. Firth

National Research Council of Canada, Ottawa

A linear gate will have better coupling characteristics if two, rather than one, metal oxide semiconductor field effect transistors are used. With two complementary MOS FET's in parallel, spikes that occur from the turn-on pulse being fed through the gate-drain capacitance are cancelled, and the input signal can be cleanly transferred to the input. The circuit is useful in multiplexing or sample-and-hold applications.

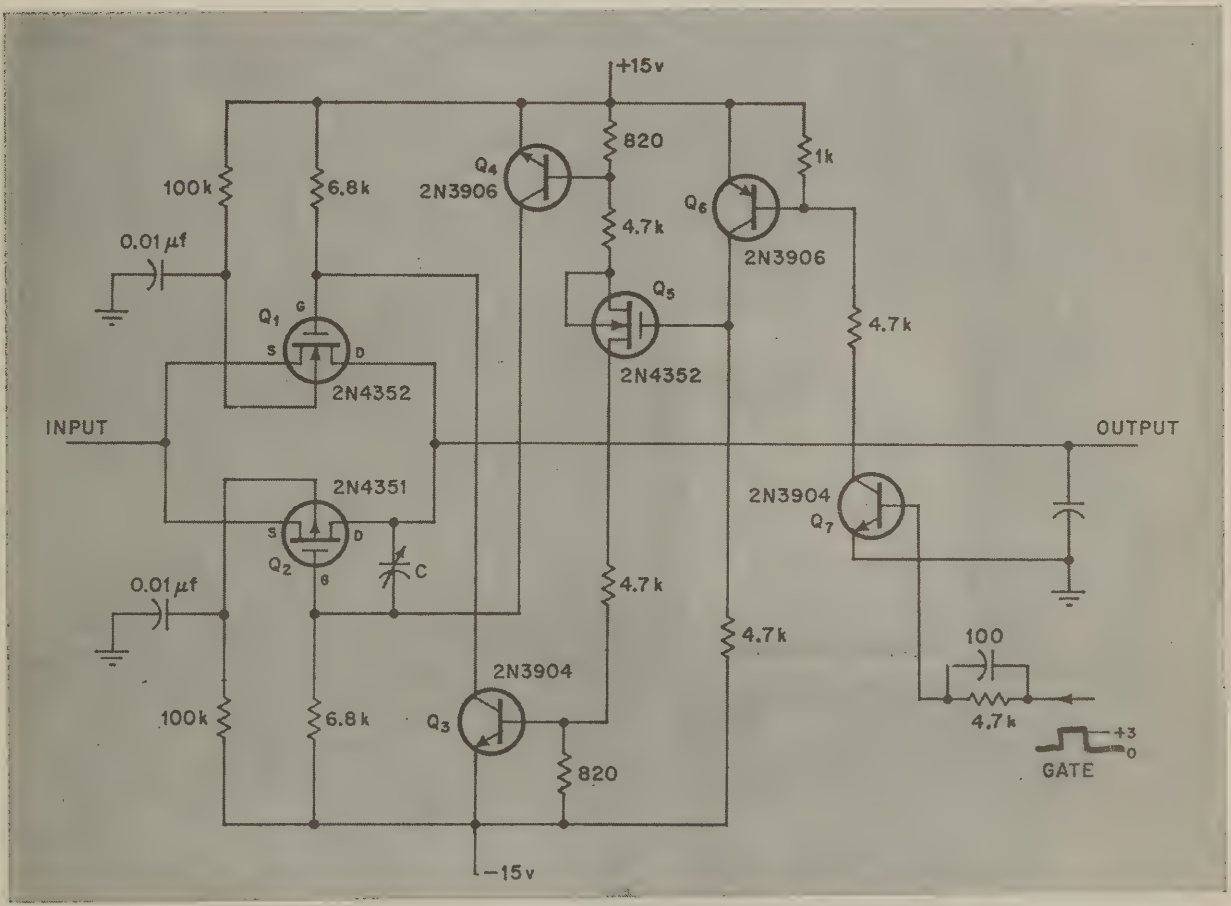
Transistors Q_1 and Q_2 form the complementary series linear gate. They are normally held off by a reverse bias applied to their gates. In addition, the substrates are reverse-biased via the 100-kilohm resistors and are decoupled to ground. This helps minimize parasitic feedthrough.

A positive pulse is applied to transistor Q_7, turning it on; in turn, Q_6 and Q_5 are switched on. Q_5 generates equal and opposite drive currents to turn on Q_3 and Q_4, thus driving Q_1 and Q_2 at the same rates and assuring that transients generated by each MOS FET will cancel each other.

The capacitor C is a trimmer which can be adjusted to null any remaining transients that might occur from circuit asymmetry.

The gate's switching speed depends on the value of resistors R_1 and R_2; for higher speeds R_1 and R_2 should be decreased. The circuit is useful for sampling times down to 100 nanoseconds. The input voltage range is ±10 volts and can be increased by increasing the supply voltages. The capacitor at the output is selected according to the holding time desired and the sampling time available.

The on-resistance of the linear gate is less than 200 ohms and the off-resistance is greater than 10 megohms.



Throughput. The signal to be transmitted is fed to MOS FET's Q_1 and Q_2 simultaneously and transferred out when the two transistors are switched on. A positive pulse at Q_7's input turns it on; in turn, Q_6 and Q_5 are switched on. Q_5 turns on Q_4 and Q_3, which, in turn, bias the two MOS FET's into conduction.

DTL/TTL controls large signals in commutator

By Francis J. Honey
Denver Research Institute, Denver, Colo.

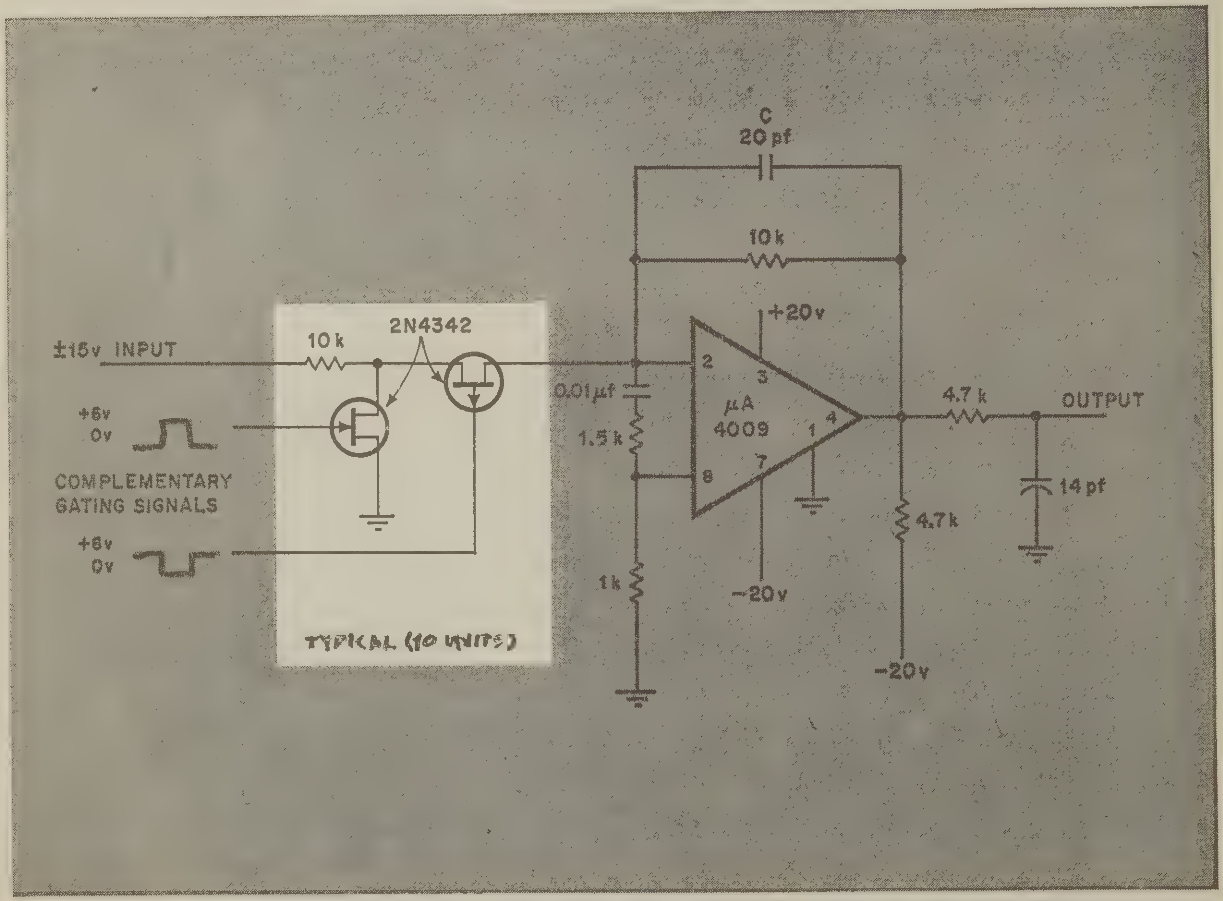
Two field effect transistors inserted at the virtual ground input of an operational amplifier allow high-voltage inputs to be switched by standard diode-transistor logic or transistor-transistor logic gates. Up to 10 pairs of FET switches can be connected together for commutating many input signals.

For the gating signal to switch the FET, the gate's voltage must exceed the sum of the applied signal voltage and the FET's pinchoff voltage. To accomplish this, two FET's are used. FET Q_2 is inserted at the virtual ground of the op amp, assuring a minimum switched signal voltage when the FET is turned on. The second FET, Q_1, provides the proper action in the off condition to insure that the input signal isn't transmitted during this interval.

When Q_2 is gated on, the input signal is fed to the amplifier, but the virtual ground from Q_1 makes the input signal very small and therefore allows Q_2 to be held off by a gating signal only slightly larger than its pinchoff voltage. The maximum signal voltage that can be switched is limited only by the maximum signal swing of the op amp and its slew rate. Ten pairs of FET switches may be stacked to produce a 10-input commutator. The switches can be driven by DTL or TTL logic if the FET is chosen to have a pinchoff voltage less than 5 volts.

The maximum commutation rate is limited by the slew rate of the amplifier, 10 volts/second for the 4009. Thus signals can be switched at a rate of 100 kilohertz.

The RC low-pass filter has been inserted at the output of the amplifier to reduce switching transients that can arise from the gate-drain capacity of the FET's.



Times ten. Complementary inputs from either diode-transistor logic or transistor-transistor logic can be used to switch field effect transistors Q_1 and Q_2 on or off and allow high-input signals to be passed by the op amp. A stack of ten FET switches can be used to commutate input signals at up to 100-kilohertz rate.

Capacitors add up in voltage multiplier

By H.R. Mallory

Mallory Battery Co., Tarrytown, N. Y.

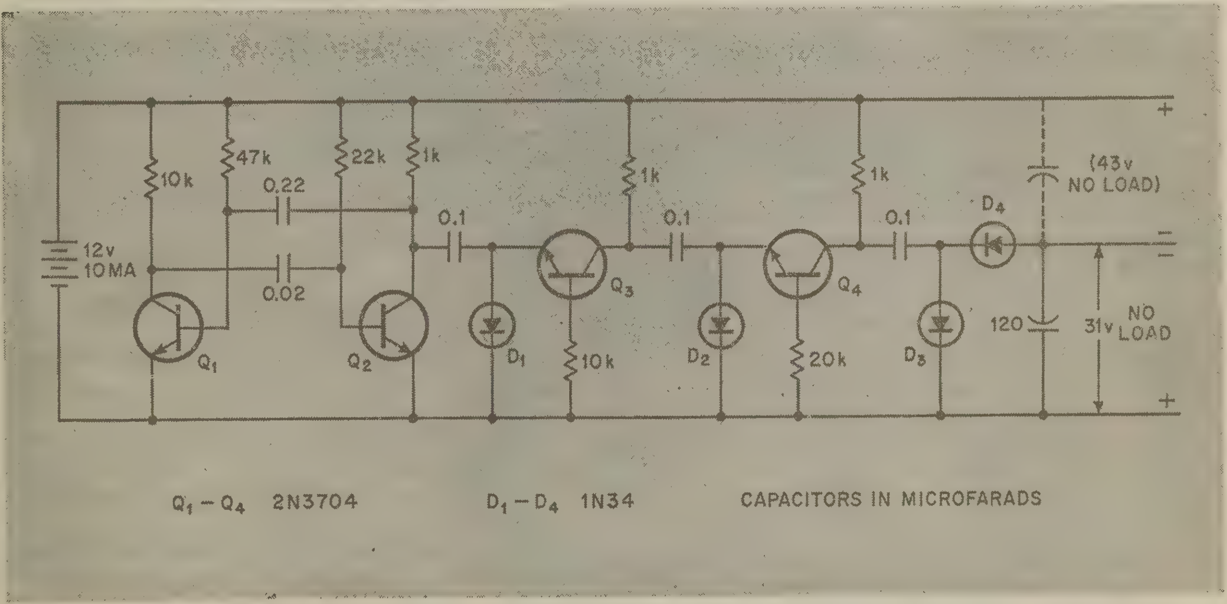
By charging several capacitors in parallel and then discharging them in series, an output capacitor can be charged to essentially a multiple of the supply voltage. The circuit is useful in building transformerless d-c to d-c converters, where any number of stages can be added to produce a desired voltage ratio. Using a transformer may require custom-tailoring for a special turns ratio.

The circuit produces an output voltage almost triple the supply voltage. Transistor Q_2, which is part of a free-running multivibrator, switches off and on at a frequency determined by the component values of the multivibrator. When Q_2 is off, the three 0.1-microfarad capacitors charge to the supply voltage less the forward drop of the diodes through the 1-kilohm resistors and the diodes. Transistors Q_3 and Q_4 also remain off—they are reverse-biased by the diodes' forward voltage drops.

On the next half-cycle of the multivibrator, Q_2 turns on, and the capacitors forward-bias Q_3 and Q_4 into conduction. The capacitors are connected in series-aiding as their charge is transferred through diode D_4 to the 120-μf output capacitor. The voltage to which an unloaded output capacitor charges is about three times the supply voltage minus the voltage drops of diodes D_1 through D_4, and the saturated voltage drops of transistors Q_2 through Q_4.

Diode D_4 prevents the output capacitor's charge from leaking when transistor Q_4 is off and the last multiplier capacitor again is charging to the supply voltage.

By referencing the output capacitor voltage to the positive side of the supply line, an extra stage of multiplication is gained. A multivibrator frequency of 1,350 hertz was used to provide 31 or 43 volts across the 120-μf capacitor. With a different number of multiplication stages, other multiples of the supply voltage will be obtained. And the circuit can be tailored to operate at other supply voltages as well as at different switching frequencies.



Series-aiding. When transistor Q_2 is off, the three 0.1-microfarad capacitors charge to the supply voltage. On the next multivibrator cycle, Q_2 turns on, also turning on transistors Q_3 and Q_4. The three capacitors, now in series, unload their charge on the 120-μf output capacitor which charges to triple the supply voltage.

A staircase and a ramp yield multiple sawtooths

By Eric G. Breeze

Fairchild Semiconductor, Mountain View, Calif.

Sawtooth waveforms are used for character generators in cathode-ray tube displays and for sweep circuits in oscilloscopes. Several waveforms generated in synchronism and occurring sequentially can be made with a combined analog and digital circuit. The digital segment generates a staircase whose equal-amplitude steps are added algebraically to the ramps of a sawtooth generator—the analog portion. The sum adds up to a sawtooth whose period is the length of the staircase.

Many applications have to resort to motor-driven potentiometers to generate long, sequential sawtooths. However, these potentiometers are not always reliable. This circuit generates sawtooths with long periods (in seconds) where the amplitudes track over large temperature variations.

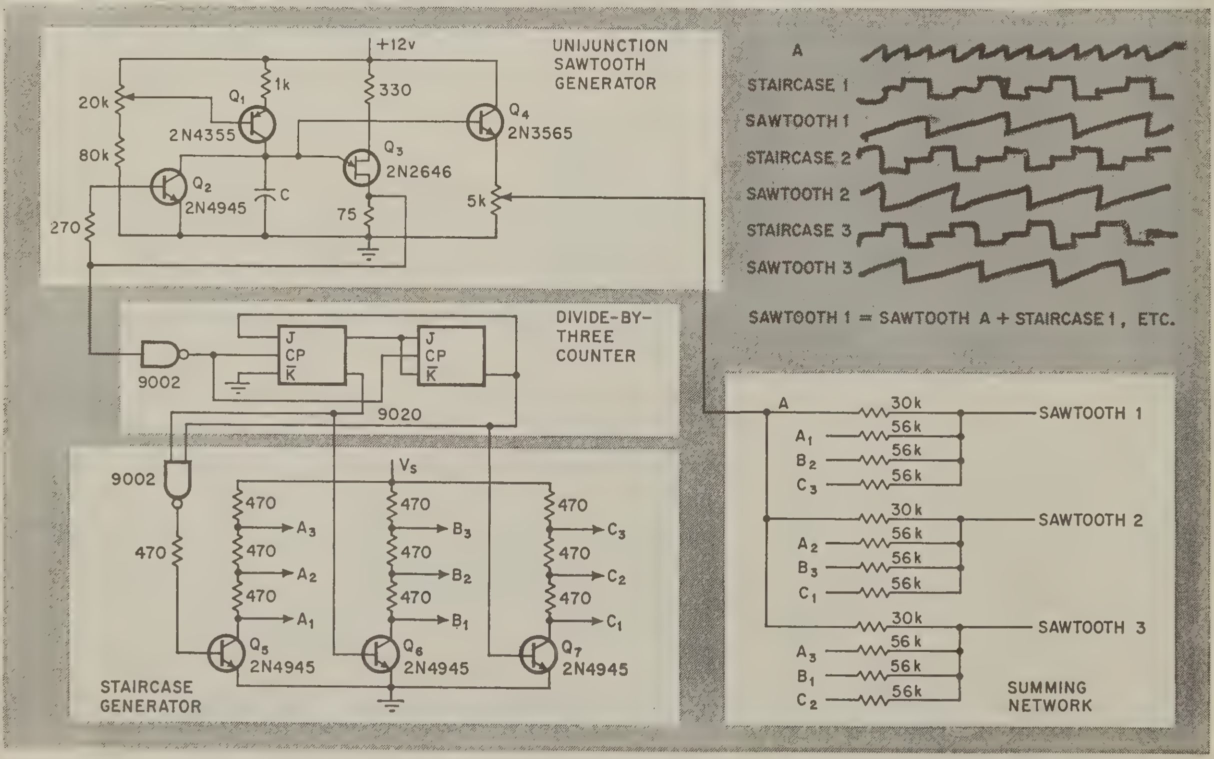
The circuit can be divided into four functional parts: a unijunction transistor sawtooth generator, a divide-by-three flip-flop circuit, a transistor staircase generator, and a resistive summing network.

Transistor Q_1 acts as a constant-current source which linearly charges the capacitor C to the unijunction transistor Q_3's firing voltage. Transistor Q_2 functions as a quick discharge path during the sawtooth's flyback time. The sawtooth generated at the unijunction's gate is transmitted to the resistor summing network through the emitter-follower, Q_4, which provides a low output impedance.

When the unijunction fires, the divide-by-three counter, 9020, is clocked, and the decoded counter outputs sequentially switch on transistors Q_5, Q_6, and Q_7 of the staircase network. The transistors' load resistors are connected in series as three equal resistances. When any of the three switching transistors conduct, a different voltage is generated at each of the the three resistor nodes. The voltages are 0, ⅓, and ⅔ of the supply voltage, V_s.

By connecting the summing resistors with the transistor loads, sequential staircase waveforms are generated. And when the sawtooth is summed with the staircase, long sawtooths are generated with periods equal to the length of the staircase.

Only three sequential sawtooths are shown here, but the number can easily be extended through the same techniques. Transients occurring in the output due to switching can be easily filtered.



Summed up. The unijunction circuit produces a sawtooth that goes to the resistor summing network. Pulses from the circuit also trigger the divide-by-three counter which gates the staircase generator (Q_5, Q_6 and Q_7). The staircase is summed with the waveform, producing a sequential sawtooth output.

Variable d-c input adjusts pulse width over wide range

By S. Nagarajan

Hindustan Aeronautics Limited, Hyderabad, India

A triangular-wave generator connected to one of the differential inputs of a comparator forms the basis for a simple pulse-width modulator. When a modulating signal is applied to the comparator's other input, the circuit will develop a train of output pulses with widths proportional to the amplitude of the modulating signal.

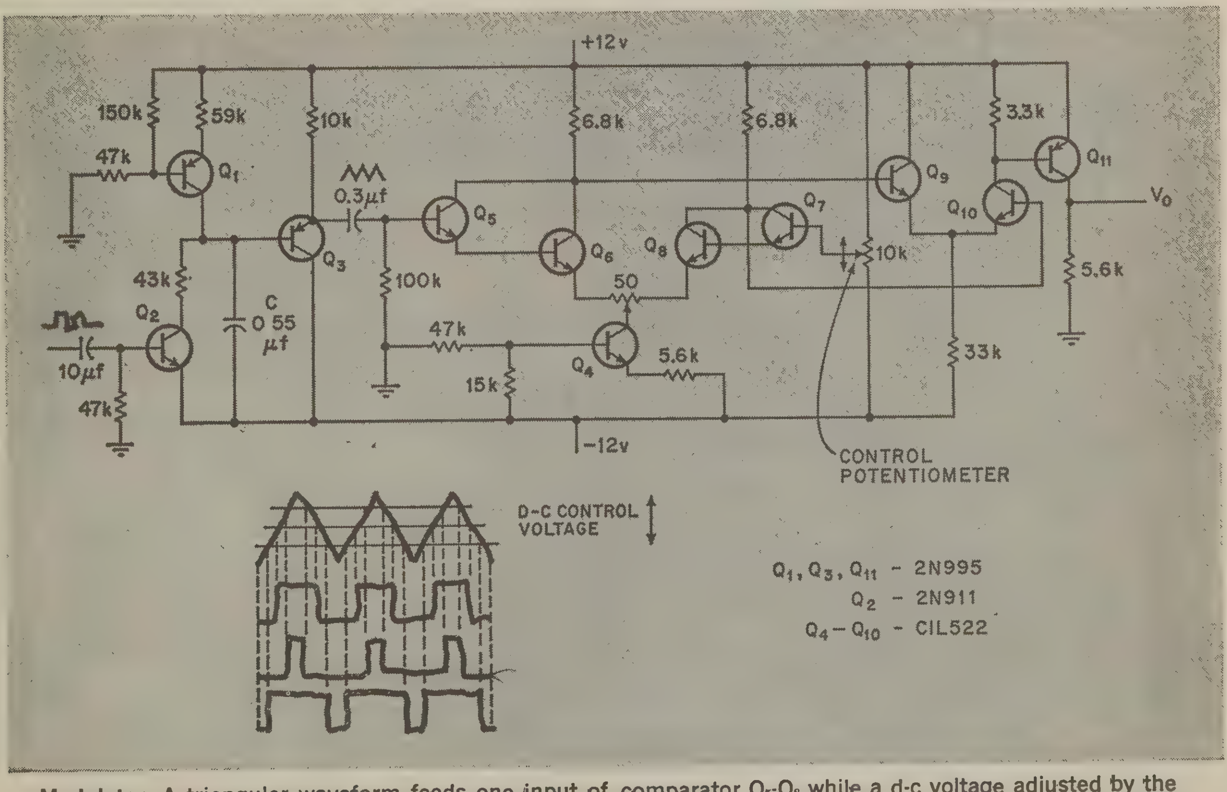
The simplest case uses a d-c voltage as the modulating signal. The mark-space ratio of the pulse train can be varied by varying the d-c input voltage.

The triangular wave is generated during the linear charging and discharging of capacitor C. The capacitor is shunted by transistor Q_2, which is turned on and off by an input square wave. When the transistor is off, the constant-current generator Q_1, charges the capacitor; when the switch is turned on, the capacitor discharges through Q_2. If the collector load of Q_2, which establishes the discharge time constant, is properly chosen, the discharge can be made almost linear; the result will be a triangular wave. The emitter follower, Q_3, delivers the wave to one input of the comparator.

The magnitude of the control voltage or modulating signal is adjusted by the 10-kilohm potentiometer and is applied at the other input of the comparator. If the voltage set by the potentiometer at the base of Q_7 is less than the voltage generated by the triangular wave at Q_5's base, current from the constant-current generator, Q_4, flows through Q_5 and Q_6, lowering Q_9's base voltage relative to Q_{10}. Hence, Q_{10} conducts while Q_9 remains off. The current flowing in the collector load of Q_{10} causes Q_{11} to saturate, producing a 12-volt output pulse for the time that the voltage of the triangular wave is greater than the d-c control signal.

When the triangular wave drops below the modulating signal, the reverse procedure occurs. Q_7 and Q_8 conduct, lowering the base voltage of Q_{10}, which shuts off while Q_9 conducts. With Q_{10} off, Q_{11} also is biased off, and the output across the 5.6-kilohm resistor drops to ground.

The circuit was designed to operate at a frequency of 100 hertz, but scaling the integrating capacitor's value will produce lower or higher frequencies.



Modulator. A triangular waveform feeds one input of comparator Q_5-Q_8 while a d-c voltage adjusted by the 10-kilohm pot feeds the other. When the d-c voltage exceeds the triangular voltage, Q_{10} and Q_{11} are off and the output is 0 volts. When the reverse occurs, Q_{10} and Q_{11} conduct and the output rises to 12 volts.

Feedback circuit checks thermal resistance

By Paul Cade

International Business Machines Corp., Essex Junction, Vt.

Thermal resistance between two points usually can be determined by measuring the power dissipated through the thermal path and the temperatures at the path's two end points. But gauging a transistor's junction-to-case thermal resistance presents a problem: although collector dissipation and ambient temperature can be measured easily, checking the actual junction temperature is difficult. This measurement can be avoided if two, instead of one, ambient temperatures and associated power dissipation readings are taken under a constant junction temperature.

Thermal resistance in this case is

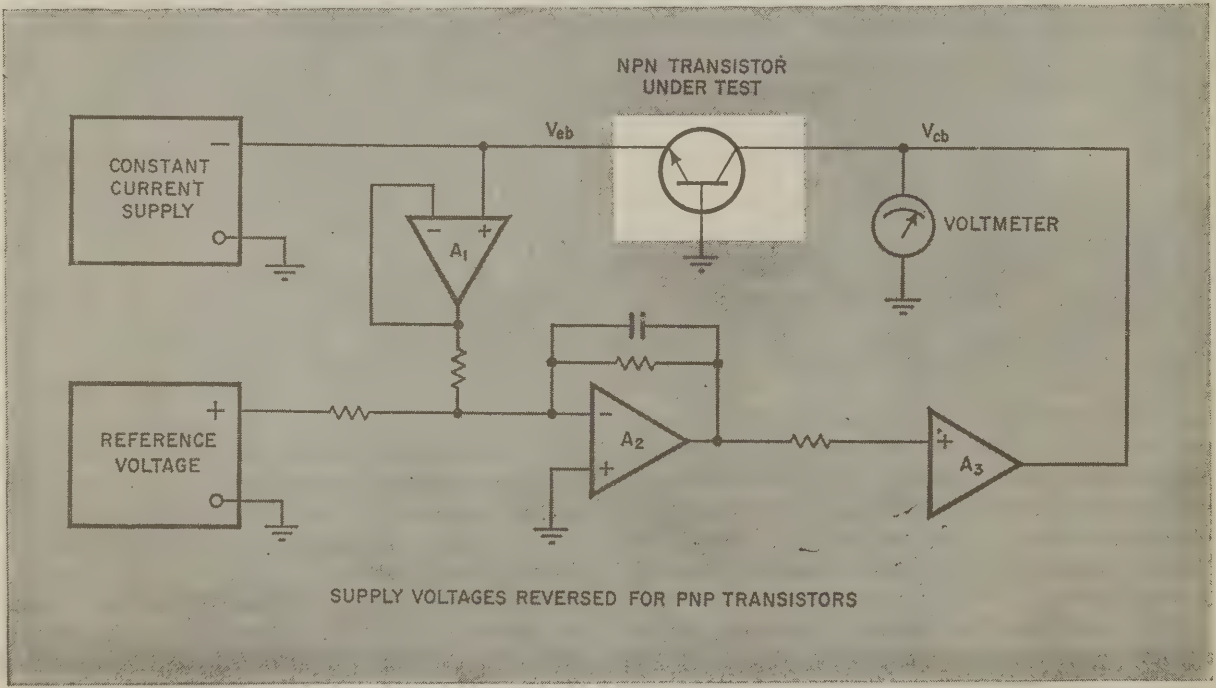
$$\theta_{jc} = \frac{T_{A1} - T_{A2}}{I_e(V_{cb2} - V_{cb1})}$$

where T_{A1} and T_{A2} are ambient temperatures, I_e is emitter current and V_{cb2}, and V_{cb1} are collector-base voltages.

With constant current, the voltage drop across a forward-biased p-n junction (in this case, the transistor's base-emitter junction) is a decreasing function of temperature. However, if voltage is kept constant through a feedback arrangement, the base-emitter junction temperature of the transistor will remain constant, regardless of ambient temperature changes, as will the temperature of the nearby collector-base junction.

Thus, by varying collector voltages to maintain constant emitter voltage on the transistor in different temperature environments, junction temperature can be maintained fairly accurately and the thermal resistance can be determined from the given equation.

In the feedback circuit, both the constant-current supply and the reference voltage are adjusted for the desired emitter current and voltages for a particular transistor family. The transistor is immersed in a temperature-regulated water or oil bath and V_{cb} is noted. Then the transistor is immersed in a second bath, the new V_{cb} is noted, and the tempera-



Measuring up. The transistor is immersed in two different temperature baths while maintaining a constant emitter current. The feedback circuit senses changes in V_{eb} from the reference voltage, driving V_{cb} so that it increases the collector-base junction temperature. This, in turn, drives V_{eb} back to nominal value.

tures and voltages are substituted into the equation to obtain θ_{jc}.

A decrease in the emitter-base junction temperature will cause a rise in V_{eb}, which is sampled by a high input-impedance, unity-gain amplifier, A_1. This, in turn, feeds the summing junction of A_2, where the signal is compared to the reference voltage. The error between the reference voltage and the increasingly negative V_{eb} (when $T_{A1} > T_{A2}$) is inverted by A_2. A_2's signal drives a power amplifier, A_3, which drives V_{cb} to a greater positive voltage. The increasing V_{cb} causes an increase in the collector-to-base junction temperature, due to greater power dissipation. This, in turn, drives the emitter-base temperature up and V_{eb} back to its nominal value. The operator does not have to readjust the V_{cb} each time the transistor is placed in a new temperature environment.

Large batch-type measurements can be automated by recording the V_{cb} on tape or cards.

Zener diode in op amp's loop enables symmetrical clipping

By Raymond Liu

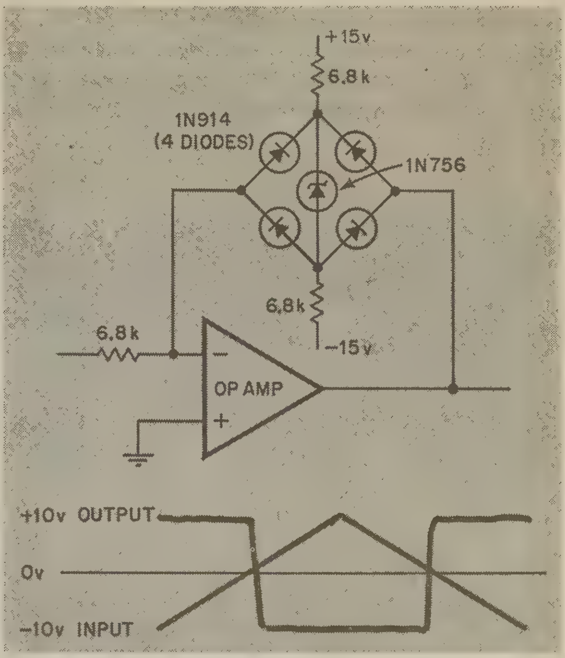
Perkin-Elmer Corp., Norwalk, Conn.

An operational amplifier, with a bridged zener diode network in its feedback loop, clips and squares the edges of a-c inputs with fast transitions each time the zero crossover of the a-c input signal is detected. The circuit is especially useful in phase-sensitive demodulation networks.

The common approach that employs back-to-back zener diodes in the feedback path of the op amp is less effective because of the decreased circuit gain that occurs when the diodes operate below the knee of the zener curve at low input signals. Often, the pulse transitions are unsymmetrical for leading and trailing edges, and the rise and fall times are slower.

In the bridged network, positive amplitudes of the input generate a negative pulse, while negative inputs generate a positive voltage level.

The zener diode provides a stable floating-reference voltage with the aid of the positive and negative supply voltages and the two 6.8-kilohm resistors. When the amplifier saturates, the two terminals of the zener are connected to the summing node and output of the op amp. Since a stable voltage across the zener can always be established without reducing the op amp's high forward gain, the circuit will produce symmetrical hard-amplitude clipping with sharp zero crossover, even at low input signals.



Stable. The feedback network provides a stable floating reference without reducing the op amp's high forward gain. Sharp zero crossovers result.

IC's gate FET's for roll rate data

By W.A. Cooke

Lockheed Missiles and Space Co., Sunnyvale, Calif.

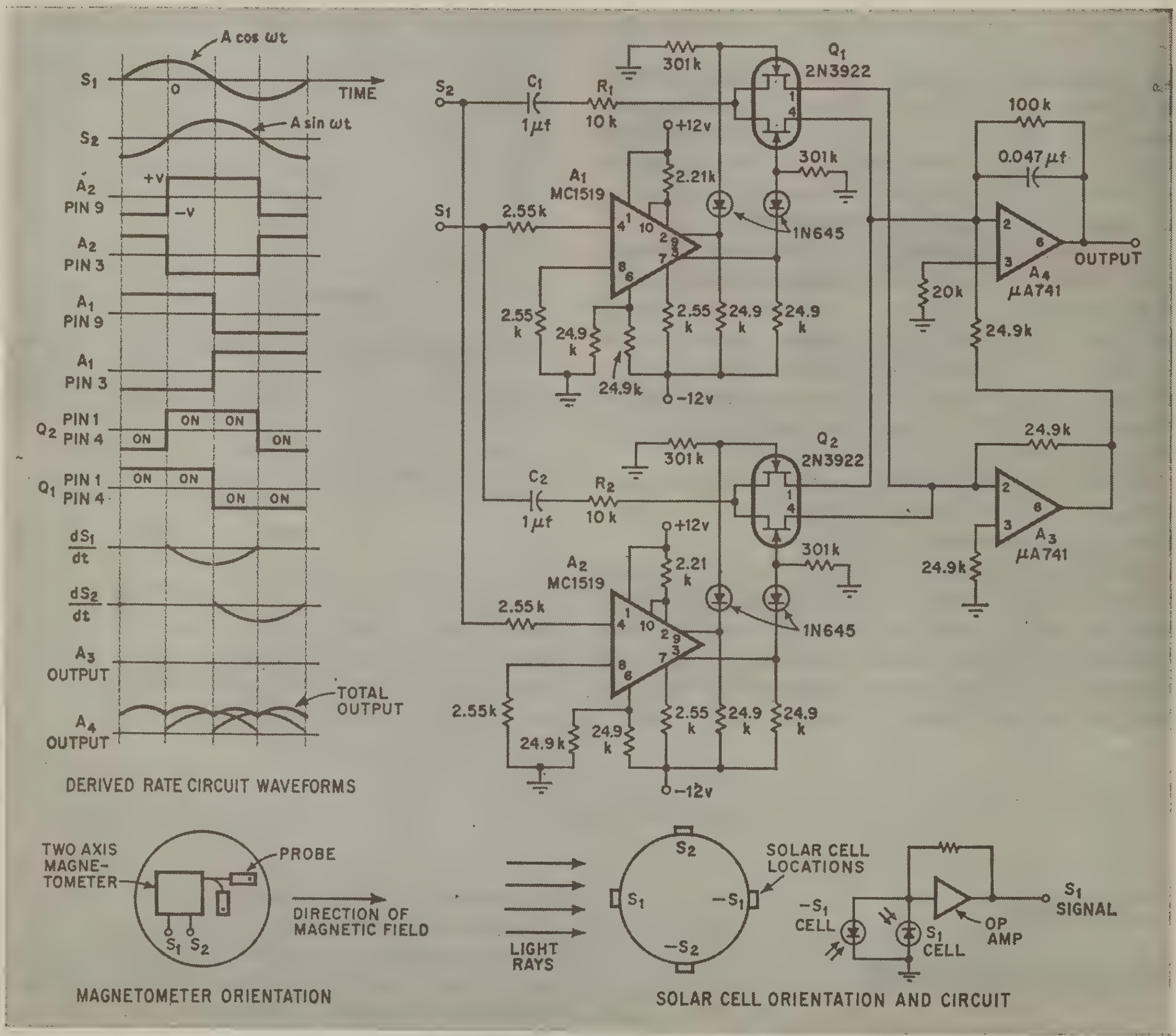
Electromechanical gyroscopes, used to stabilize the flight of space vehicles, are expensive and consume a great deal of power. An electronic counterpart, made of reference sensors, IC amplifiers, and field effect transistors, eliminates these two problems. In addition, the electronic version is a much lighter package.

The circuit, called a derived-rate circuit, generates an output voltage that corresponds to the roll rate of the vehicle. Sensors—either solar cells or magnetometers—provide input information for the circuit. As the vehicle rolls, the sensors, which are located in quadrature around the perimeter of the vehicle, generate a sinusoidal wave whose frequency is proportional to the roll rate of the vehicle. The waveforms are combined and converted to yield an output voltage with a scale factor of 0.1 volt per radian per second.

In the derived-rate circuit, the sinusoids arriving at the S_1 and S_2 inputs are 90° out of phase with each other and have constant amplitudes. Two input signals are differentiated to produce new signals whose amplitudes are proportional to the angular frequency ω and shifted 90°. Hence, this voltage is dependent on input frequency or spin rate of the vehicle. Only the negative-half cycles are inverted by an amplifier and then summed with the positive-half cycles to produce the output waveform shown below.

The two input IC's, MC1519's, are differential amplifiers which clip the input sinusoids and use them as gating signals to the field effect transistors, Q_1 and Q_2. At the same time, the two sinusoids from S_1 and S_2 are differentiated by the networks, R_1–C_1 and R_2–C_2, to generate the frequency-dependent relation. The differentiated signals are delivered to the source of the dual FET's. The positive-half cycles of the differentiated S_1 and S_2 signals are channeled by Q_1 and Q_2 directly to the output amplifier A.

Negative-half cycles of the differentiated signals are channelled by Q_1 and Q_2 through inverting amplifier A_3. The amplifier inverts the negative cycles of the differentiated signals and feeds them to the output amplifier where they are summed with the positive cycles.



In a spin. Sensors located on the rocket's periphery generate input sinusoidal waves which are amplified and gated to produce a nearly constant output voltage corresponding to the rocket's roll rate. The output is made up of positive- and negative-half cycles of the input after they are differentiated and rectified by the circuit.

A dynamic load tester for regulated power supplies

By Robert D. Guyton

Mississippi State University

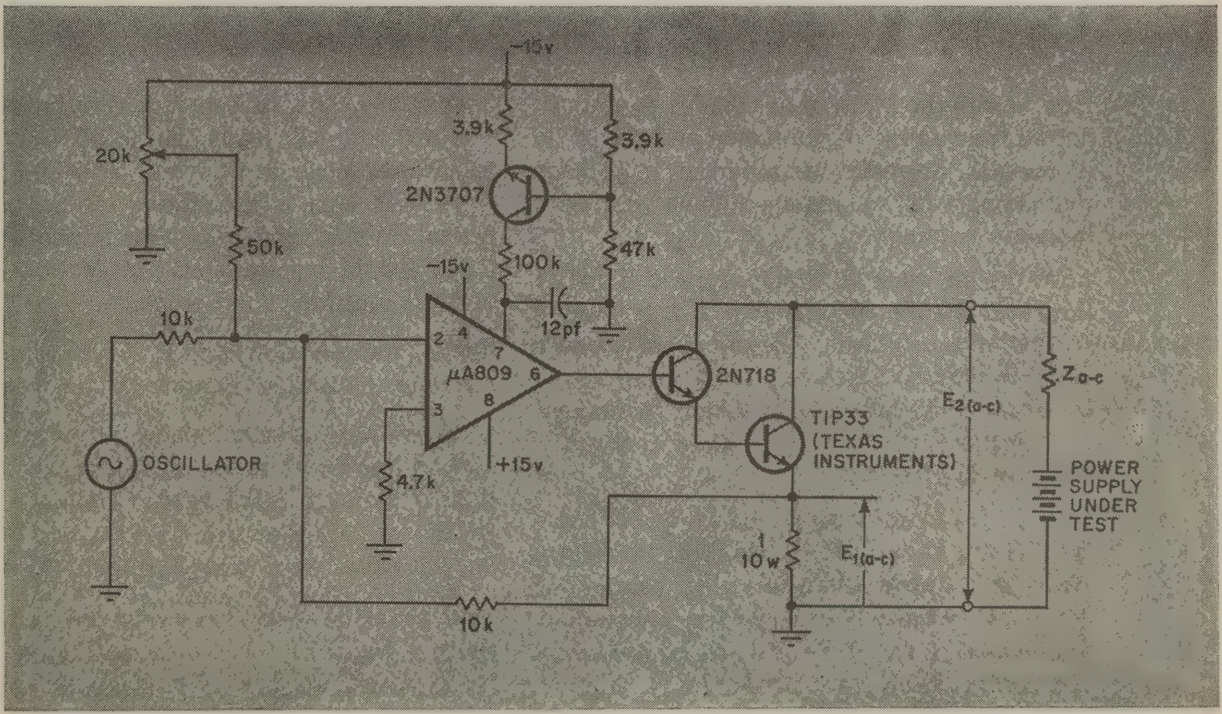
The dynamic output impedance of a regulated power supply can be measured by a high-gain feedback amplifier that accurately sets the a-c load current over a broad frequency range. The circuit is useful for measuring the power-supply impedance as a function of frequency or in displaying the voltage-current characteristic from no load to short circuit on an oscilloscope.

The input to the operational amplifier consists of two components: an a-c component from the oscillator and a d-c component set by the 20-kilohm potentiometer. The pot controls the amount of d-c current drawn from the power supply. Since the a-c voltage across the 1-ohm resistor is proportional to the a-c current through it, the impedance of the power supply can be obtained simply by calculating the ratio E_2/E_1, where E_1 is the peak-to-peak voltage across the 1-ohm resistor and E_2 is the peak-to-peak voltage across the power-supply terminals. The best way of determining the ratio is by using a dual-channel oscilloscope.

The feedback amplifier assures a stable response over a large frequency range. For small signals in the range of 50 ma, the circuit can measure impedances at frequencies up to 500 kilohertz.

The circuit connected to pin 7 of the op amp improves its high-frequency large-signal response without lowering its gain appreciably.

To measure the voltage-current characteristics of the power supply from no load to short circuit, the input amplitude of the oscillator is made sufficiently high to drive the power transistor at 100 hz. The voltages generated at E_1 and E_2 are connected to the horizontal and vertical channels of the scope, and the characteristic curve on the screen can be observed.



Impedance. An a-c component from the oscillator and a d-c component from the potentiometer are delivered to the input of the op amp. The power transistor forces an a-c voltage across the 1-ohm resistor from which the power supply's impedance, Z, can be readily determined from the relation $Z=E_2/E_1$.

P-i-n diode T switch consumes little power

By Roland J. Turner

General Atronics Corp., Philadelphia, Pa.

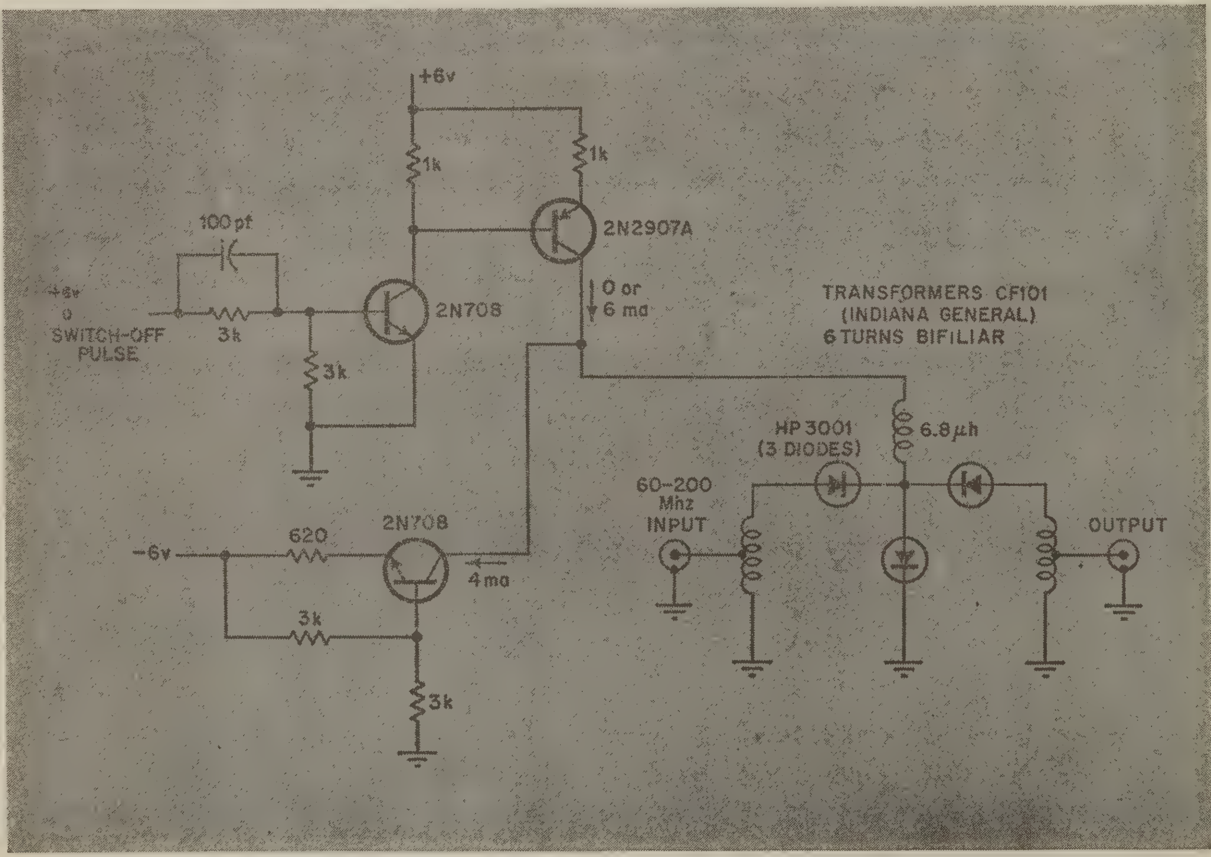
High isolation and low insertion loss is usually difficult to achieve in the familiar balanced-bridge radio-frequency switching circuits because of the voltage offset and capacity of the diodes. Better performance can be obtained with the single-ended configuration that uses three p-i-n diodes connected as a T switch. With this setup, only a small current drive of 2 milliamperes is needed for each diode, thus allowing many gates to be handled by one driver circuit at a lower power consumption than other switching circuits.

The circuit is normally on with no switch-off pulse present. Thus the two-transistor control circuit is off while the shunt constant-current circuit draws 4 ma from the diode T switch. The two back-to-back diodes in series each conduct 2 ma while the shunt diode remains off. At this current level, each conducting diode has a forward resistance of about 10 ohms, which accounts in part for the circuit's low insertion loss of 1.3 decibels at a frequency of 60 megahertz. Higher control current would decrease diode resistance but increase the needed driver power.

The T switch employs a wideband toroidal transmission-line type transformer which converts the 50-ohm transmission line characteristic impedance at the center tap to 200 ohms, thus minimizing the insertion loss effects of the diode resistance at the low control current used.

When a 6-volt positive pulse appears at the gate's input, both transistors in the gating circuitry turn on, generating 6 ma of current at the output. Thus a net current of 2 ma is forced into the diode switch, back-biasing the series diodes and forward-biasing the shunt diode. The switch opens and the signal is blocked.

At higher frequency levels the p-i-n diodes must be driven harder, turned on by 10 ma, to achieve insertion losses below 1 db and isolations in excess of 50 db at 600 Mhz.



Low bias. The T switch needs less control current and, therefore, less power to switch radio-frequency signals. In its normally on condition, the constant-current circuit draws 4 milliamperes from the diode T switch. The two back-to-back diodes are in series, with each conducting 2 ma while the shunt diode remains off.

Regulator holds temperature of chip's substrate constant

By D.P. DeAngelis and M. Palumbo

Dynell Electronics Corp., Melville, N.Y.

Many monolithic transistor arrays containing matched transistor pairs also incorporate a substrate temperature regulator on the same chip. This regulator is useful in building low-drift differential amplifiers. However, the matched transistors in the circuits now available commercially have bandwidths limited to 40 megahertz, which may not be large enough for some applications. Other arrays without the regulators, such as the RCA CA3045, have transistor pairs with bandwidths of 300 Mhz; an external temperature regulator can be built to take advantage of this wide bandwidth.

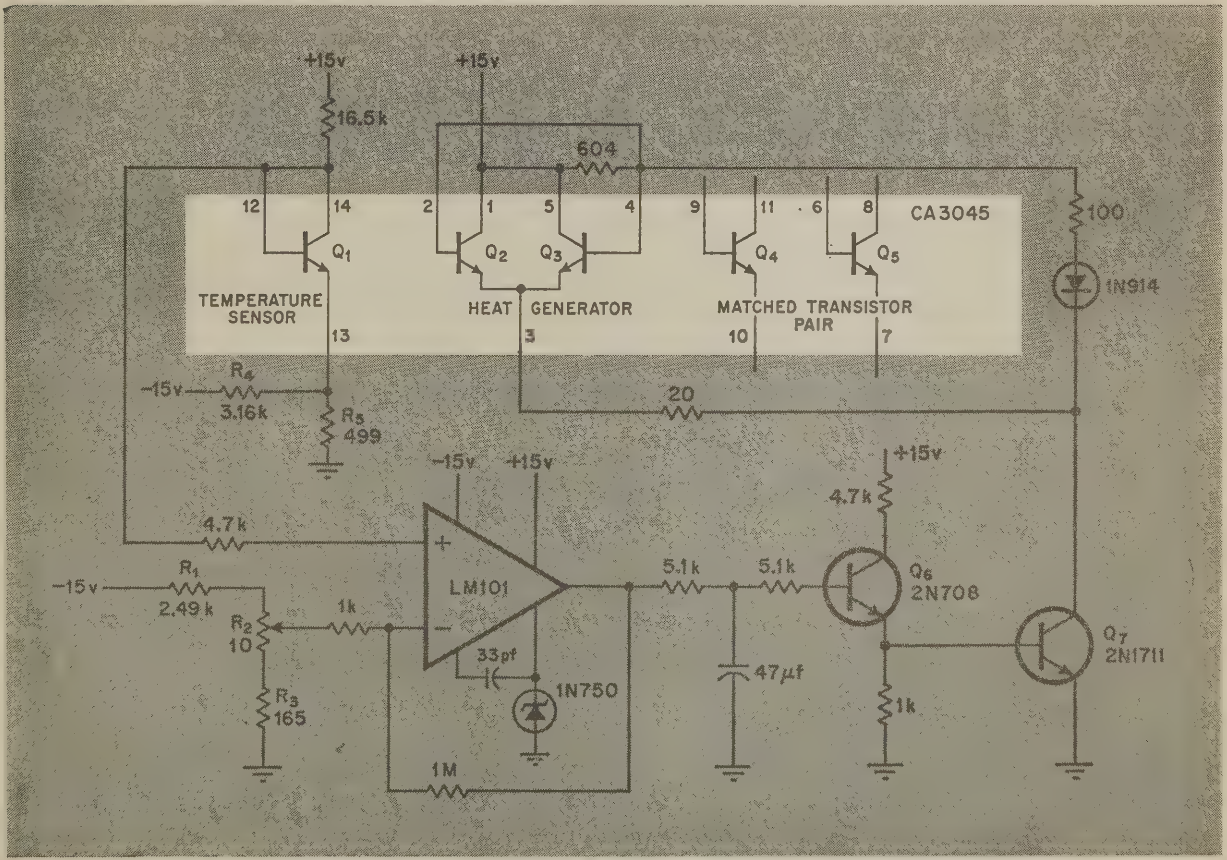
In the array, transistor Q_1 serves as the temperature-sensing element for the heated substrate; its base and collector are tied together to act as a diode. The base-emitter voltage varies linearly with temperature. Transistors Q_2 and Q_3, connected in a constant-current mode, provide the power to heat the substrate to the desired ambient temperature, and Q_4 and Q_5 are the matched transistor pair with the 300-Mhz bandwidth.

The external temperature regulator consists of the op amp—LM 101 and its associated circuitry —which detects a voltage corresponding to the substrate's temperature and compares it with a voltage set initially to correspond with the desired ambient temperature. The differences between these two voltages is amplified and delivered to Q_2 and Q_3 on the chip, which in turn heats the substrate.

The voltage divider, composed of R_1, R_2, and R_3, is set to a voltage corresponding to the maximum desired substrate temperature. When the ambient temperature goes down, the feedback from the regulator pumps more power to the chip to heat it.

The substrate is biased at —1.5 volts by R_4 and R_5 to maintain the proper p-n junction isolation between the transistors on the chip.

The circuit operates over an ambient temperature range of 0°C to 70°C. The input offset voltage of the matched transistor pair does not exceed 5 millivolts over the 300-Mhz bandwidth.



Good Match. Q_1 senses the substrate's temperature and delivers the corresponding voltage to one input of the op amp. The other input is set to the voltage equivalent of the desired temperature. This voltage difference drives the current regulator, Q_2-Q_3 which heats the chip to hold its temperature constant.

Diodes eliminate crossover distortion in video amplifier

By Roland J. Turner

General Atronics, Philadelphia, Pa.

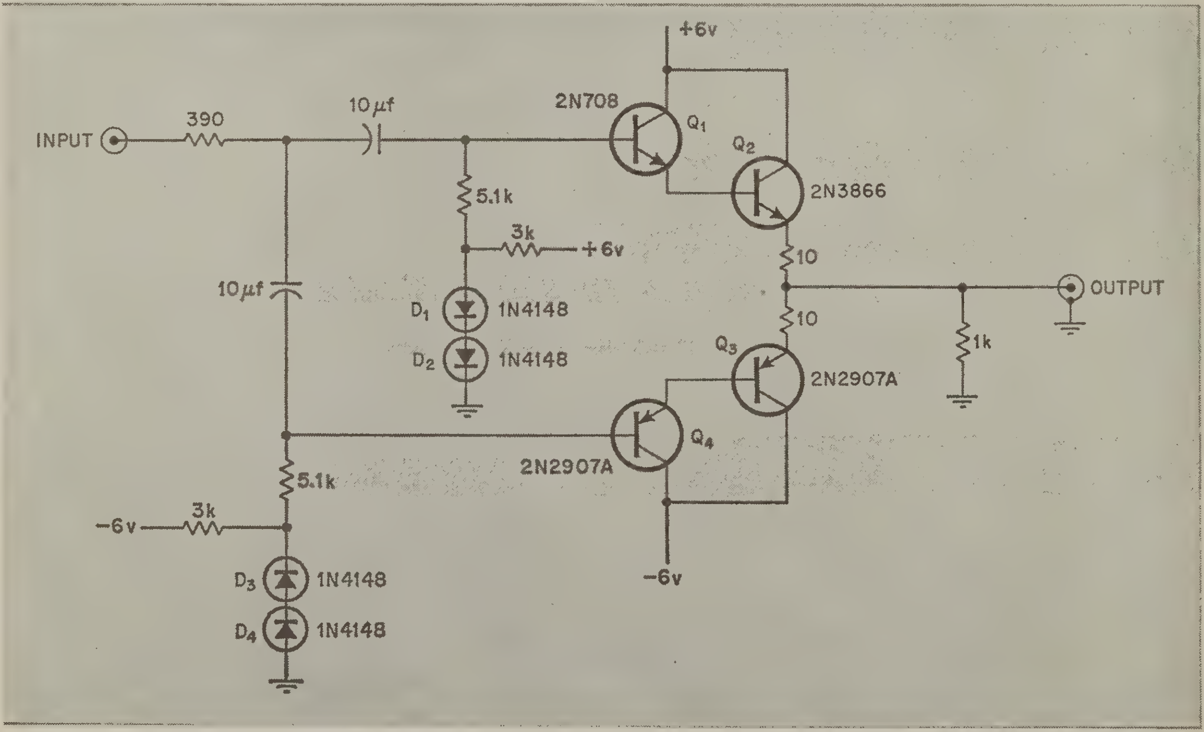
A video amplifier with a dual Darlington transistor configuration operates in a true class B manner because silicon diodes bias the transistors into immediate conduction. Unlike most resistor-biasing used in other amplifiers, crossover distortion is completely eliminated over a wide temperature range because the forward drop of the diodes tracks the forward drop of the transistors with changing temperature.

During positive signal swings Q_1 and Q_2 conduct; during negative swings Q_3 and Q_4 conduct. The result is a low output impedance for both positive and negative signal swings. Diodes D_1 and D_2 are forward-biased to provide a 1-volt d-c bias to transistors Q_1 and Q_2. This overcomes the initial forward blocking voltage across the base-emitter junctions in each transistor so that the complete positive cycle of the input signal can be transmitted. Since the same applies to the biasing of transistors Q_3 and Q_4, the full negative swing is transmitted.

The output impedance of the driver is 12 ohms at up to 2 megahertz. And 50- to 100-ohm transmission cables can have up to 100-picofarad loads and still be driven efficiently.

The video amplifier delivers 270-milliampere signal swings into a 30-ohm load at 1 Mhz. The 3-decibel cutoff frequency for the amplifier is 13 Mhz.

If the 10-ohm resistors in the emitter circuits of the output transistors are eliminated, then the output impedance of the amplifier will be 2 ohms at up to 2 Mhz with a small tradeoff in linearity.



Class B. True class B operation is obtained from the dual Darlington configuration by biasing the transistors with silicon diodes. Forward drop of the diodes temperature-track the forward drop the transistors, eliminating crossover distortion in the amplifier over a wide temperature range.

Shift register simplifies design of phase comparator

By Ivars Breikss

Honeywell Test Instruments Division, Denver, Colo.

A bidirectional shift register and one other integrated circuit are all that's required to build a phase comparator for pulse trains of varying frequencies. The register produces an output pulse pattern with a duty cycle proportional to the relative phase of the two input signals, but in contrast to other comparators, it produces no outputs if other frequency ratios are present. The relative phase between the two signals may vary over a 360° range.

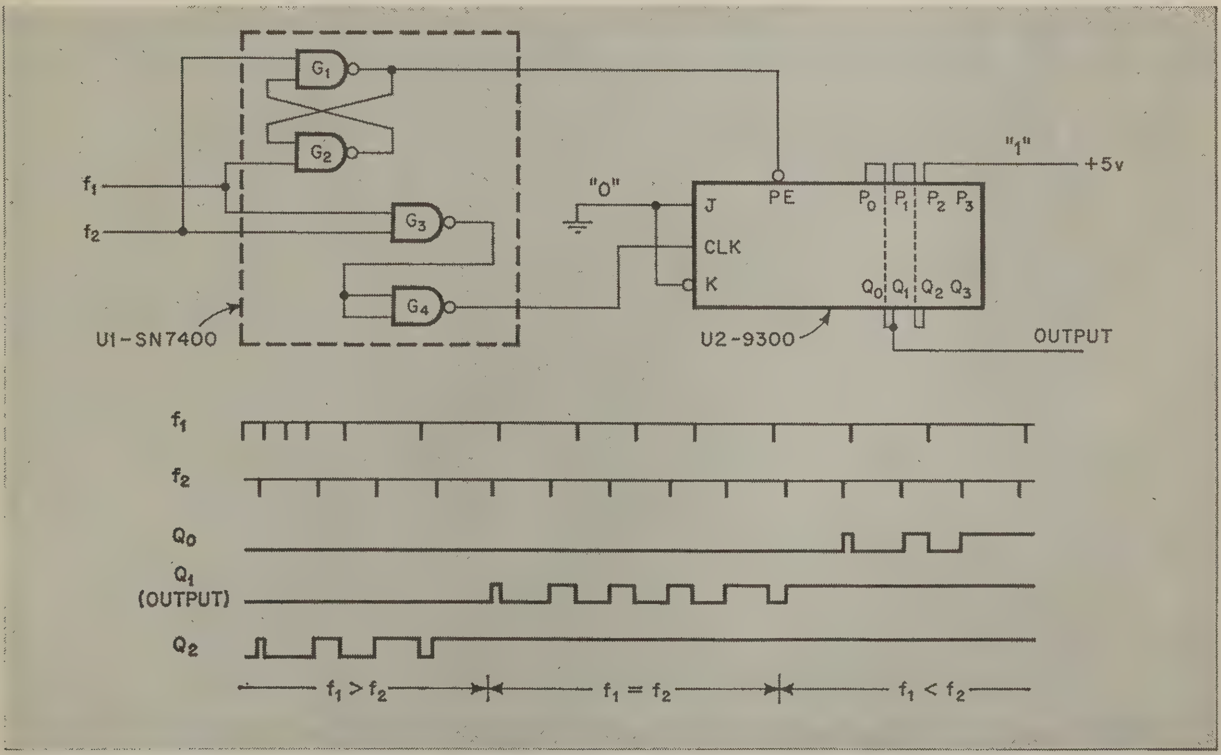
The shift register contains four bits, of which three are used. The bits in the register are shifted when the positive edge of a pulse arrives at the clock input to the register. The shift is to the right when the parallel enable input, PE, is at logical 0, and to the left when PE is a logical 1.

The shift direction is determined by the state of the flip-flop G_1 and G_2. The input signals, f_1 and f_2, trigger the flip-flop, whose output is a 1 when a pulse from f_1 occurs and is 0 with a pulse from f_2. Thus f_1 drives PE to a 1 and shifts the register 1 bit to the right, while f_2 drives PE to 0 and shifts the contents 1 bit to the left.

A 0 is continuously entered into the first bit position of the register and a 1 in the third bit position; the fourth bit is not used. A pulse from f_1 shifts the 0 to the second bit position of the register and the output Q_1 is a 0.

As long as pulses on the f_1 input arrive, or a preponderance of f_1 pulses occur, the logic state of Q_1 will remain at 0. If the f_2 pulses begin to predominate, the 1 applied at the third bit position P_2, will be shifted to the left and the output will be a constant logic 1. If the pulses at f_1 and f_2 arrive alternately, then the 0 and 1 applied at P_0 and P_2 will be alternately shifted into bit position P_1, resulting in an output containing an alternating pulse pattern of 1's and 0's. The duty cycle of the pulse pattern will indicate the relative phase—or equivalent delay—between the two input trains of the same frequency.

Appropriate filtering at the output provides a d-c level proportional to the phase difference between f_1 and f_2 when the two frequencies are equal. A maximum or minimum voltage indicates one of the other modes of operation.



Right shift. The middle-bit position, P_1, of the shift register will alternate between logical 1's and 0's when the two input signals, f_1 and f_2, are equal in frequency. The duty cycle will be proportional to the phase difference between the incoming pulses.

IC line-receiver converts pulses to logic levels

By Ken Erickson

Interstate Electronics Corp., Anaheim, Calif.

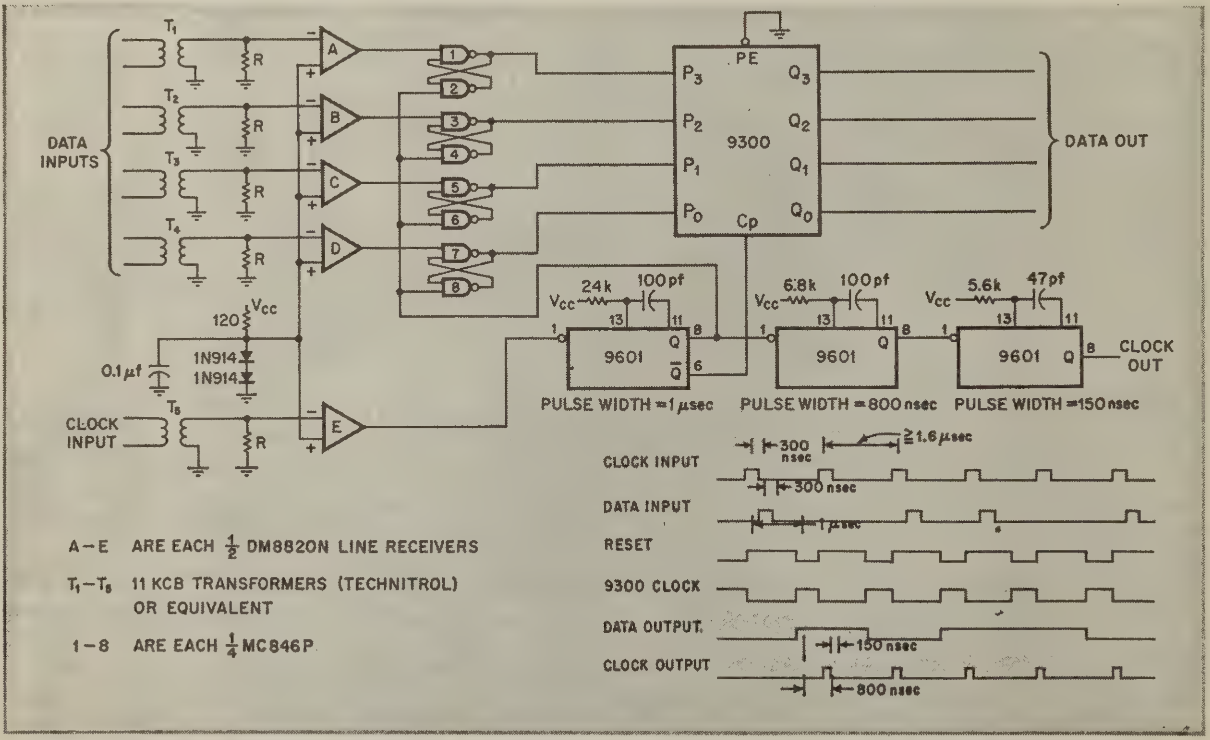
When digital data is transmitted over long distances, use of transformer coupling is desirable for maintaining isolated signal grounds at opposite ends of the transmission line. But because the data is in true-and-false, constant-voltage, logic levels, the pulse transformers cannot handle this data format. Thus the data must be transmitted by short pulses accompanied by clock pulses. Because of differences in transmission line and driver delays, timing problems often ensue. However, a digital data line receiver using integrated circuits can convert the data and clock pulses back to the original data format of logic levels, while allowing a generous tolerance on the skew deviation between pulses.

The receiver is equipped for four input data channels and one clock channel, but can be expanded to handle more data channels. One 9300 register would be required for each additional four bits added. Each data channel contains an IC line receiver and a latch made with a pair of NAND gates that temporarily store the incoming data. Before a clock pulse arrives, all the latches are held in the reset mode by one of the complementary outputs of the 1-microsecond, one-shot multivibrator. The reset signal is removed when the one-shot is triggered. A latch is set whenever a data pulse is received on one of the input channels; otherwise the latch remains reset.

The 9300 register is clocked on the trailing edge of the 1-μsec pulse from the one-shot, transferring the data stored in the latches to the register.

The two other one-shots in the circuit generate a 150-nanosecond output clock which is delayed by 800 nsec with respect to a change in the output data. The delay eliminates any race conditions between the clock and data outputs wherever the two signals are used.

The circuit receives four channels of data at a rate of 600 kilohertz with a nominal pulse amplitude of 5 volts and a pulse width of 300 nsec. The resistor R should have a value that matches the characteristic impedance of the coax or twisted-pair transmission line. The input threshold voltage is about 1.4 volts and is obtained by forward-biasing two 1N914 diodes.



Delayed. Each pair of NAND gates forms a latch which is held in the reset mode prior to the arrival of an input clock pulse. The pulse triggers a 1-μsec one-shot while the incoming data pulses set the appropriate latches. Then the 9300 register stores the data transferred from the latches.

Op amps reject line noise in a-d converter's input

By Dusan Velasevic and Srdan Stankovic

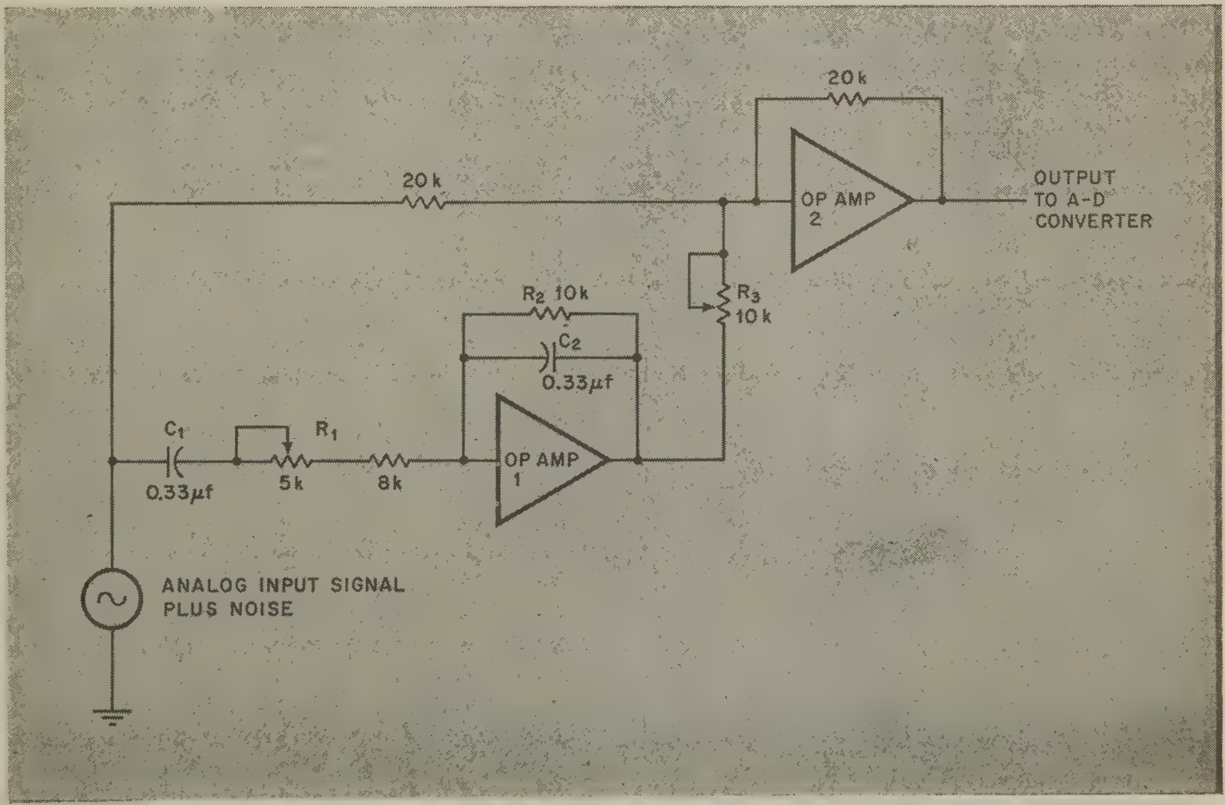
Institute of Nuclear Sciences, Belgrade, Yugoslavia

Line frequency noise from analog signals can considerably reduce the accuracy of output signals from an analog-to-digital converter. But two operational amplifiers can be used to separate and filter noise from analog signals before conversion without appreciably prolonging settling time.

The input signal, comprising the line frequency noise superimposed on the analog signal, is fed simultaneously into the two op amps. The high-pass R_1C_1 network at the input of the first op amp filters out the analog portion and, with adjustment of R_1 and R_2C_2 keeps the phase shift of the noise through the first op amp constant. This op amp inverts the noise waveform.

The second op amp acts as a summing network for the analog input signal, its noise component, and the inverted noise component passed by the first op amp. The summing network thus actually subtracts out the noise component. Potentiometer R_3 can be adjusted to provide complete cancellation of the line frequency noise.

By comparison, when a Gaussian three-pole active filter is incorporated into an a-d converter to reject noise, the converter's settling time is 200 milliseconds at 0.01% of full scale. The op amp circuit's settling time is 40 milliseconds with the same rejection ratio and line frequency noise.



Fast conversion. The second operational amplifier sums the signal plus noise with the inversion of the noise transmitted from the first op amp network. The output thus comprises only the analog signal, which is then fed to the analog-to-digital converter.

Resistors come to light in digital display system

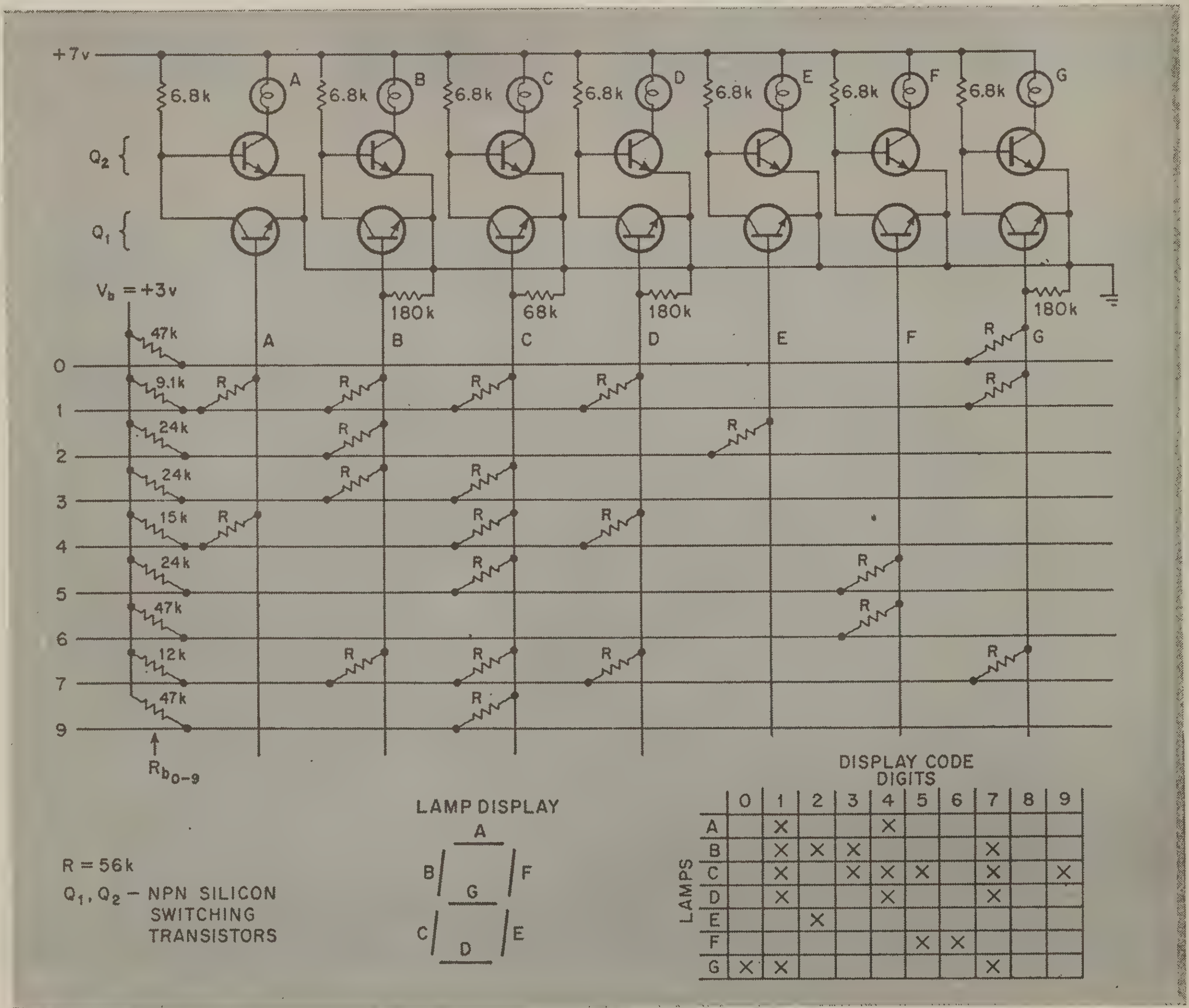
By R.K. Sharma

Instrumentation Limited, India

A seven-segment digital display system built with a resistor matrix is less costly and far more reliable than a system built with a conventional diode matrix. Cost and reliability advantages are attributed to the fact that fewer components are used (21 resistors versus 49 diodes).

And unlike the conventional diode system, the newer system's lamps glow when there is no active input to the terminals. When a particular digit is to be displayed, unwanted lamps are extinguished by a voltage applied to the digit's input terminal. In the conventional system, the diodes distribute the current needed to drive the transistors that turn on the lamps for the desired digit. But with the new system, high-value resistors are used so that the current delivered to undesired transistors are small enough to be negligible. The input terminals of the matrix take signals from a decoder that converts the binary-coded decimal numbers of a binary counter into decimal numbers.

To extinguish a digit's lamp, a voltage greater than the supply, V_b, must be applied at the digit's input terminal. The current generated by V_b and the input voltage passes through the resistors, R_b, and arrives at the bases of transistors, Q_1, through the resistors R. Transistors not connected to the active input through an R resistor are unaffected. This current is enough to saturate the Q_1's, whose



LAMPS	0	1	2	3	4	5	6	7	8	9
A		X			X					
B		X	X	X				X		
C		X		X	X	X		X		X
D		X			X			X		
E			X							
F						X	X			
G	X	X						X		

Resistive. The voltage applied at the input terminal turns on the transistors, Q_1, connected to the terminal by the resistors, R. Transistors, Q_2, turn off and extinguish the desired lamps. Below is the display code that shows which lamps must be out to display a particular digit.

low saturation voltage keeps the transistors, Q_2, off and, consequently, the lamps off.

The remaining terminals are kept slightly below the threshold voltage of transistors Q_1, since V_b by itself is not high enough for turn-on. Thus Q_1's collector-emitter voltage in the off state saturates its respective Q_2. Hence, these lamps all glow.

To display a 0, its input voltage is raised higher than the threshold of the input transistor to lamp G, turning it on. This, in turn, cuts off the following transistor stages, extinguishing lamp G.

Input terminals 1 to 9 are at a voltage below threshold and, therefore, the current delivered to the corresponding transistor bases will be insufficient to drive these transistors into saturation. Therefore, the Q_2's corresponding to these input terminals will be on. Thus, lamps A, B, C, D, E, and F keep glowing and the digit 0 is lit.

To light the digit 8, all lamps must glow. Thus, no input terminal is needed for this digit.

Unijunction controls oscillator in simple underwater pinger

By Frank Watlington

Columbia University Geophysical Field Station, Bermuda

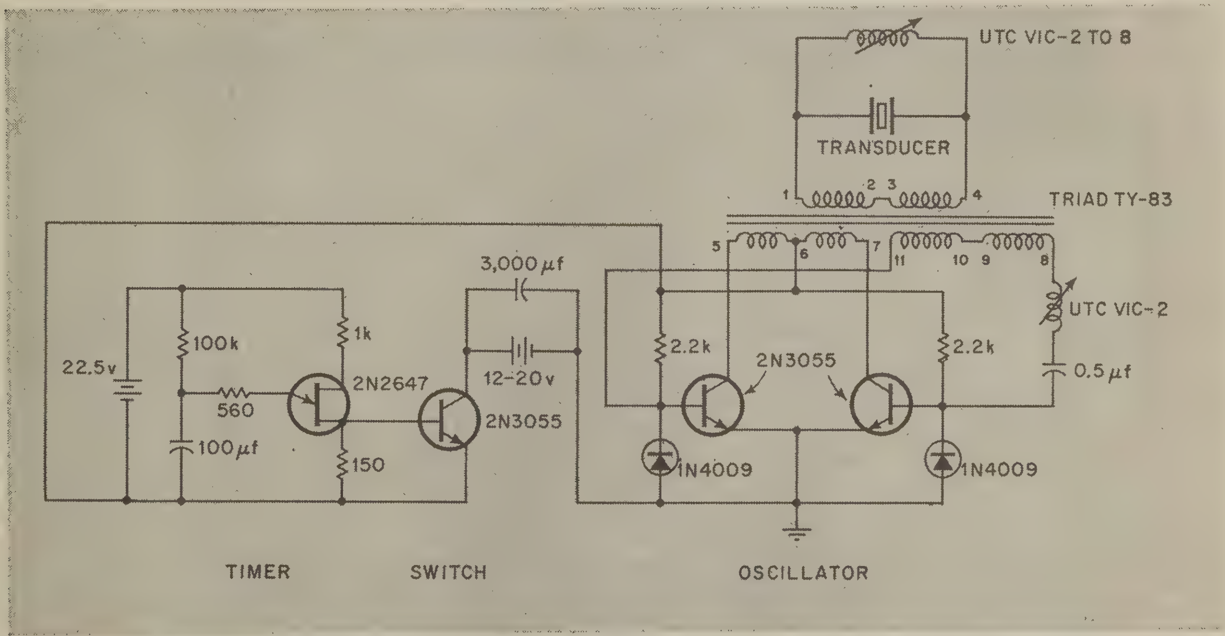
An oscillator, timer, and switch connected to a transducer produce a simple device called an oceanographic pinger. The unit can be used to produce sound waves underwater.

A pulse from the unijunction transistor timing circuit turns on the 2N3055 transistor switch which applies power to the oscillator circuit. The timer controls the duty cycle (and, consequently, the life of the flashlight batteries used to power the oscillator). The unijunction circuit's repetition rate is determined by the 100-kilohm resistor and the pulse length by the 560-ohm resistor in series with the unijunction's emitter resistance.

Oscillator pulses are applied to the inverter transformer which steps up their voltage and applies the pulses to the transducer. The unit is tuned through the two variable inductors.

The value of the components is for operation at about 2 kilohertz, but by varying the inductors in the feedback and transducer circuits, frequencies as high as 16 khz can be obtained. If a pressure potentiometer replaces the 100-k resistor in the timing circuit, ping rate can vary with water depth.

The transducer used is a double bilaminar piezoelectric ceramic unit.



Making waves. The oceanographic pinger generates sounds underwater at a particular frequency. Pulses from the oscillator are stepped up in voltage to drive the transducer. Sound waves generated by the transducer have a frequency which can be adjusted by varying the inductors.

Other McGraw-Hill Books for Electronics Engineers

(See inside front cover for more titles)

ELECTRONIC FLASH, STROBE

By HAROLD E. EDGERTON, *Institute Professor Emeritus, Massachusetts Institute of Technology*

384 pages, 209 illustrations

Everything you need to know about today's electronic flash — whether for your work in professional photography, in research, or as a hobby — is included in this authoritative book by a leading world expert on the subject. You are given theoretical *and* practical information that guarantees you better photographs through numerous techniques developed by Dr. Edgerton and now widely used in commerce and industry. He describes typical systems employed today, plus some of the more unusual and interesting uses in science, assuring you a thorough understanding of what the techniques can mean to you. To anyone who must learn quickly and expertly about electronic flash, the book is a clear guide to all the fundamentals by the man who pioneered in the creation of the modern stroboscope.

INTEGRATED ELECTRONICS

By RODNEY SORKIN, *Electronic Engineer, U. S. Department of Defense*

224 pages, 147 illustrations,

Here is the first book to assemble all the essential elements of integrated electronics into one compact reference. It not only covers the *whole* technology—components, construction techniques, circuit characteristics, and design principles — but gives equal weight to both *fabrication* and *applications*. In this way, you get a clear working knowledge of the technology not available in any other book, and most particularly of the various factors and limitations that affect your own specialty. Whether you use it to brush up on the field, get a better grasp of the theory, or as a design aid — you will find it the most useful work of its kind in print. Thoroughly up to date, and putting emphasis where you want it, the book gives you a revealing new perspective on a rapidly expanding technology.

RADAR HANDBOOK

Edited by MERRILL I. SKOLNIK, *Superintendent, Radar Division, U.S. Naval Research Laboratory, Washington, D.C.*

1,200 pages, 1,140 illustrations

A clear, complete picture of all modern radar design techniques, applications, and concepts is offered in this world's first one-volume handbook on radar engineering. 51 top radar experts have contributed their know-how and experience to this superb reference, which provides full, accurate information on radar subsystems, radar techniques, analysis of performance, signal management, environmental effects, and system applications. In view of its enormous range of subjects covered, no matter whether you are involved with radar in air traffic control, police speedometers, or astronomy, here is a single book that will be of invaluable aid in solving any technical problem you may meet, whatever your specialization. A perfect on-the-job reference for men who need to know radar applications and concepts from other specialties.

PLASTIC COATINGS FOR ELECTRONICS

By JAMES J. LICARI, *Supervisor, Research Division of the Advanced Chemistry Laboratories of Autonetics, Materials and Processes Laboratory*

400 pages, 130 illustrations

Available at last — a practical, one-volume guide to the selection and specification of plastic coatings. This new book combines theoretical and practical data on plastic coatings for both commercial and military electronic applications. It proceeds from a discussion of basic chemistry and properties of coatings, to functions, manufacturing technology, and specific electrical applications such as printed circuit boards, resistors, capacitors, and similar devices, and concludes with a detailed survey of types of specifications used in obtaining and applying coatings. Numerous tables and lists provide instant access to data on coating properties, specifications, and tests. Clear cut graphs, diagrams, and examples offer added facts and figures at a glance.

CIRCUIT DESIGN FOR AUDIO, AM/FM, AND TV

Prepared By THE ENGINEERING STAFF OF TEXAS INSTRUMENTS INCORPORATED

352 pages, 7⅛ x 9⅞, 145 illustrations

Stressing time- and cost-cutting approaches, this practical volume is packed with proven new procedures for solving typical problems in audio, AM/FM, and TV circuit design. With examples and procedures illustrating the latest available transistor devices, it covers such important topics as design of IF strips, neutralized and unneutralized amplifiers, IF amplifier designs for AM/FM and FM IF amplifier circuit applications, specific design examples for each major TV receiver system, UHF and VHF tuners, sync separators, vertical oscillators, video amplifier systems, TV automatic gain control, and more.

HANDBOOK OF MATERIALS AND PROCESSES FOR ELECTRONICS

Edited by CHARLES A. HARPER, *Aerospace Division, Westinghouse Electric Corporation*

1,344 pages, 803 illustrations

An indispensable working tool for all engineering and technical personnel in the electronics and electrical industries, this handbook offers the greatest wealth of basic data and applications guidance ever assembled in a single volume. 21 top specialists give you the kind of guidelines you need for all major materials and processes you use on the job, and whether you are engaged in design, development, assembly, or related activities in the electronics or electrical industries, you will turn to this massively complete handbook again and again for practical, on-the-job guidance. It will not only save you time and money, it will help you produce a better, more marketable product. Hundreds of tables, drawings and photographs.

TRANSISTOR CIRCUIT DESIGN

Prepared By THE ENGINEERING STAFF OF TEXAS INSTRUMENTS INCORPORATED

523 pages, 7⅛ x 9⅞, 526 illustrations

You can solve your circuit design problems quickly and accurately with the help of this authoritative guide which translates the most frequently used elements of transistor theory into practical solutions and gives you a large number of circuit examples with clear, easy-to-follow design procedures. It classifies all commercially available transistors, showing their relationship to each other and to the five basic fabricating techniques. It shows how to interpret data sheets and device numbers, illustrates equivalent circuits, details techniques for measuring transistor characteristics, and demonstrates the application of transistorized circuitry to air navigation, radar, remote control, and other areas.

ELECTRONIC DIGITAL TECHNIQUES

By PAUL M. KINTNER, *Manager, Digital Systems and Products Development, Industrial Systems Division, Cutler-Hammer.*

315 pages, 6 x 9, 215 illustrations

Here is a down-to-earth approach to digital systems geared to the needs of the practicing engineer. Non-mathematical in presentation, this practical guide is concerned only with actual design problems and the techniques for their solution. All of the most up-to-date methods are used. Written in an easy-to-understand style, the book is ideal for self-study. It uses algebra or other mathematical formulations only when they specifically contribute to a design technique. All topics are carefully developed — with numerous illustrations and examples — making the volume as comprehensive as possible. A large number of self-testing problems have also been included for this purpose.

Use the attached order card or write to:

Dept. 23-A191-2000-1/McGraw-Hill Book Company/P.O. Box 400/Hightstown, N.J. 08520